Eliminate VCXO Modules with New Clock Jitter Cleaners

LMK04000 Family Provides Sub-200 fs Jitter Using a Simple External Crystal

Introduction

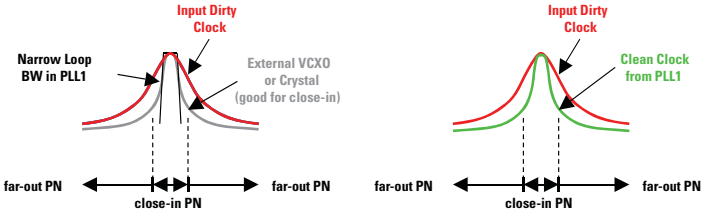
National's next generation LMK04000 Family of Precision Clock Conditioners improve system performance and accuracy. Using a new cascaded PLLatinum® architecture combined with an external crystal and varactor diode, the LMK04000 family provides sub-200 femtosecond (fs) Root-Mean-Square (RMS) jitter. The LMK04000 family is ideal for clocking Analog-to-Digital converters (ADC), Digital-to-Analog Converters (DAC) and other high-performance components used in wireless infrastructure, test and measurement, and medical ultrasound and imaging equipment.

Cascaded PLLatinum PLL Architecture

The cascaded architecture consists of two high-performance PLLs, a low-noise crystal oscillator circuit, and a high-performance Voltage Controlled Oscillator (VCO). The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock generation.

First Loop

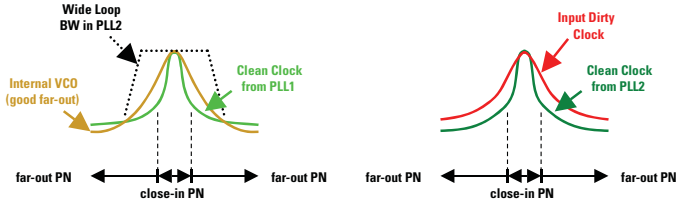
PLL1 can be configured to either work with an external VCXO module or use the integrated crystal oscillator with an external crystal and a varactor diode. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO or the crystal to clean the input clock.



Cleaning of Close-In Phase Noise in PLL1

Second Loop

The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO or crystal used in PLL1.



Cleaning of Far-Out Phase Noise in PLL2

Clock Distribution

The output from PLL2 is then divided and distributed to 5 differential outputs pairs. Each output pair consists of a programmable divider, a phase synchronization circuit, a programmable delay and either a Low-Voltage Differential Signaling (LVDS), Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) or Low-Voltage CMOS (LVCMOS) output driver. The LVPECL and LVDS outputs support clock rates up to 1080 MHz, while the LVCMOS outputs reach up to 250 MHz.

Advanced Clocking Features

The LMK04000 family features dual redundant inputs and an optional default-clock upon power up. The input block is equipped with loss of signal detection and automatic or manual selection of the reference clock. The default-clock is available on CLKout2 and it can be used to provide an initial clock for the Field-Programmable Gate Array (FPGA) or the microcontroller that programs the clock jitter cleaner during the system power-up sequence.

Easy-to-Use Clock Design Tool Software

New clock design tool software facilitates clock subsystem design, part selection and configuration, and phase noise simulations and analysis.

For more information on the LMK04000 family, visit:
national.com/timing

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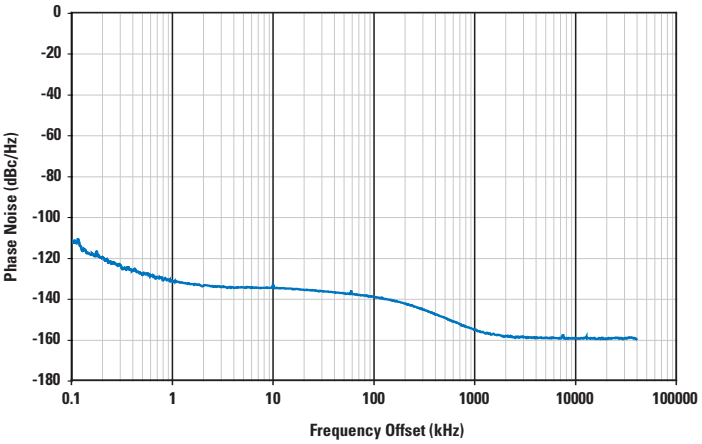
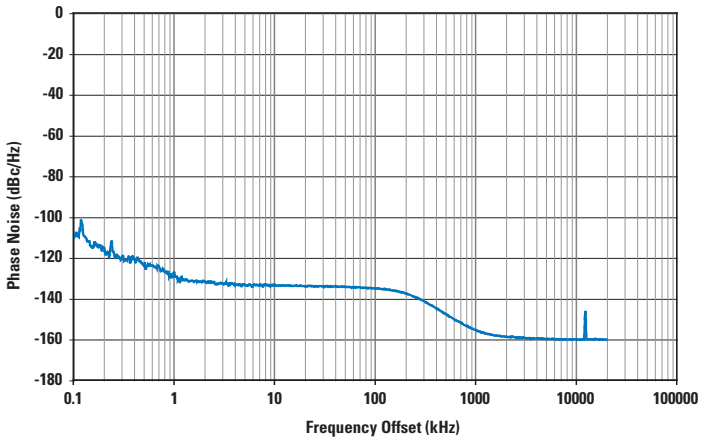
Superior Phase Noise Performance



LMK04031B LVCMOS Output Phase Noise at 122.88 MHz using a Crystek VCXO



LMK04031B LVCMOS Output Phase Noise at 122.88 MHz using a Low-Cost Vectron Crystal

LMK Family	Characteristics
LMK01000	2-input and 8-output clock buffer, divider and distributor < 30 fs of additive RMS jitter (typ) at 800 MHz Up to 1600 MHz clock frequency
LMK02000	4- and 8-outputs clock jitter cleaner, generator and distributor < 0.2 ps of RMS jitter (typ) with external VCXO
LMK03000	4- and 8-output clock jitter cleaner, generator and distributor < 0.4 ps RMS jitter (typ) integrated low-noise VCO Three performance grades (Premium, Standard, Value) Lower BOM cost and footprint using internal VCO
LMK04000	5- to 7-output clock jitter cleaner, generator and distributor < 0.2 ps RMS jitter (typ) with external crystal or VCXO Cascaded PLLatinum® PLL architecture Redundant input and default clock upon power-up Lower BOM cost using internal crystal oscillator circuit

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Design Resources

- Samples
- Evaluation kits
- Datasheets
- Evaluation board operating instructions
- Clock Conditioner Owners Manual
- CodeLoader 4
- Application notes
- NEW! Clock Design Tool Software

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