

Getting Signal Launch Right for High Speed Sub-systems

Lab Report
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Introduction

More and more video and data storage equipment is running at Gigabit rates today. They are interconnected through high speed coaxial connectors such as SMAs and BNCs. While these connectors are in general of good quality, their performance in the equipment depends on how they are mounted onto the printed circuit board. Use of a non-optimized connector footprint introduces impedance mismatches, reflections, and signal loss, and impairs the signal fidelity of the equipment. The daunting task of signal launch optimization falls into the hands of layout designers and hardware engineers who often do not have the time to get it right. This lab report outlines a few common mistakes in signal launch designs, and illustrates examples of carefully designed signal launches for edge-mount and through-hole connectors used with National's LMH0384 high-speed adaptive equalizer and LMH0307 high-speed cable driver.

Common Signal Launch Mistakes

Most connectors have large signal pins. For a connector with a 30-mil signal pin, a landing pad of 50-mil width will be necessary. 10-mil wide microstrips are commonly used for ease of routing to high pin-count integrated circuits. Board stack-up is designed to achieve a 50 Ω characteristic impedance for the 10-mil wide microstrip, with an FR4 dielectric layer of 6 mils. If the trace width is larger than 10 mils, the impedance decreases from the design target of 50 Ω . The connector's landing pad is a wide microstrip; therefore, the characteristic impedance of the pad is significantly lower than that of the trace impedance. Figure 1 is the cross-sectional diagram of the board, illustrating the phenomenon of impedance drops. The pad introduces a severe impedance drop that will impact the signal quality and add parasitic capacitance that will limit the trace's bandwidth.

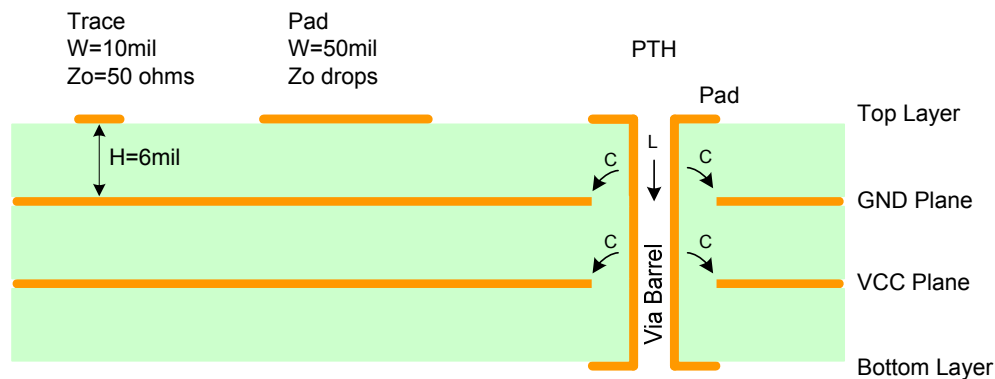


Figure 1. Cross-sectional diagram of the board

Figure 2 shows the impedance profile of an edge-mount SMA, measured with a Time Domain Reflectometer (TDR). It illustrates the huge impedance drop to 18.8 Ω caused by the large landing pad for the 50 Ω SMA. Likewise, Figure 3 illustrates the impedance drop to 37 Ω due to the large landing pad used for a 75 Ω edge-mount BNC.

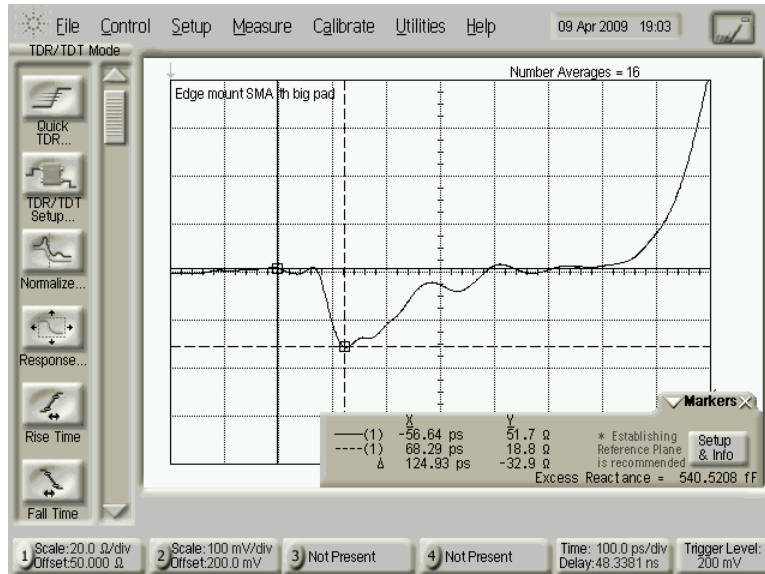


Figure 2. Impedance profile of an edge-mount SMA with large pad

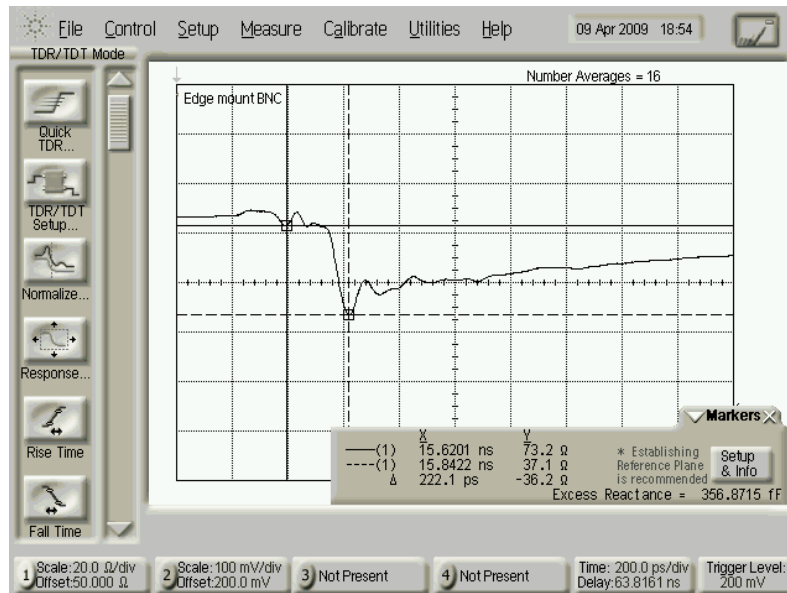


Figure 3. Impedance profile of an edge-mount BNC with large pad

Video equipment typically uses through-hole BNCs because of the better mounting robustness. These connectors are mounted onto the board with their signal pins soldered into fairly large plated-through holes and usually routed at the opposite side of the board. As illustrated in Figure 1, the inner ground and power layers are isolated from the plated-through hole to avoid short-circuit. Depending on the diameter of the hole, the cylindrical barrel introduces a certain amount of inductance. Depending on the clearance distance from the barrel, each ground or power layer introduces parasitic capacitance to the plated-through hole. With the right amount of inductance and capacitance, it is possible to create a through-hole with the desired characteristic impedance. A large plated-through hole with a small clearance will exhibit excessive capacitance that results in an impedance drop. Figure 4 shows the impedance profile of a through-hole BNC with a 60-mil hole and 20-mil clearance. It illustrates the impedance drops to 40Ω caused by the plate-through hole of a 75Ω BNC.

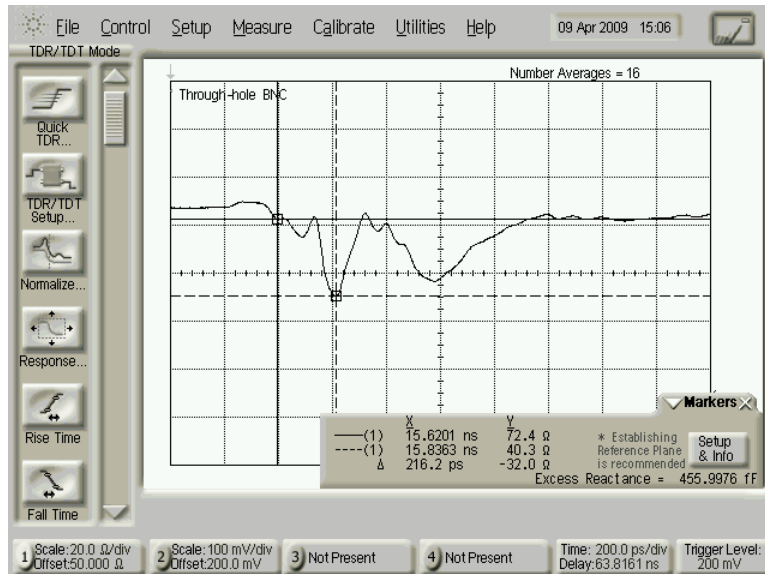


Figure 4. Impedance profile of a through-hole BNC with small clearance to ground planes

Effect of Poor Signal Launch

Why do designers have to worry about signal launch? Severe impedance mismatches cause reflections that will adversely affect the signal quality and reduce the voltage or timing margin of the data eye. Excessive parasitic capacitance of the landing pad also reduces the bandwidth of the signal path, and introduces more jitter caused by this bandwidth limitation. Figure 5 illustrates an example of a signal waveform degraded by a poor signal launch connector.

Reflection caused by poor signal launch

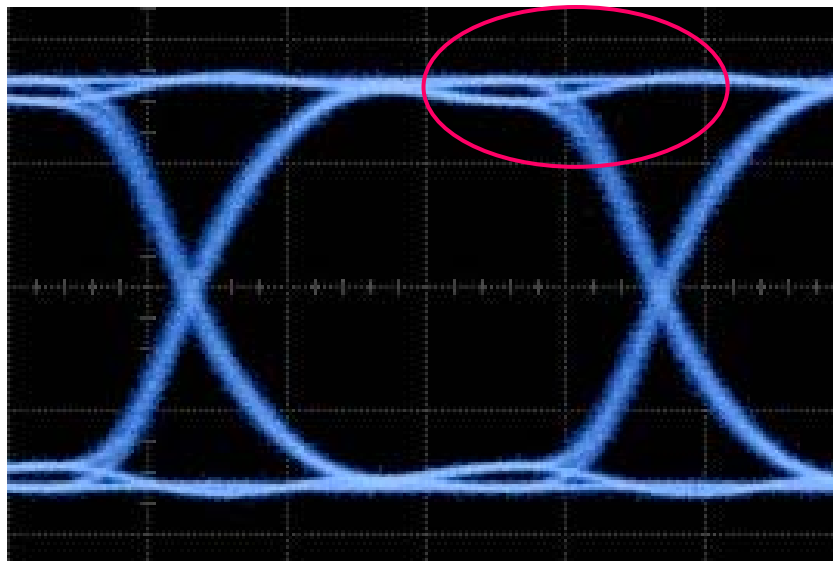


Figure 5. Signal waveform degraded by poor signal launch

Signal Launch Design - Edge-mount SMA

This section describes a signal launch design with an edge-mount SMA with a very small signal pin. In this example, it is possible to use a landing pad that has the same width as the 12-mil wide microstrip. The landing pad is transparent and is, in fact, part of the trace. The pad and the trace are expected to have the same characteristic impedance. However, in most board designs, it is common practice to use 30-50 mils clearance from metal layers to the board edge. This clearance creates a ground slot under the signal pin and will introduce a parasitic inductor at the transition from the signal pin to the board. To maintain a good signal launch, it is important to bring the pad and the ground plane under the pad all the way to the board edge. Figure 6 depicts a TDR plot that illustrates very little impedance change from the optimized landing pad used for this edge-mount SMA.

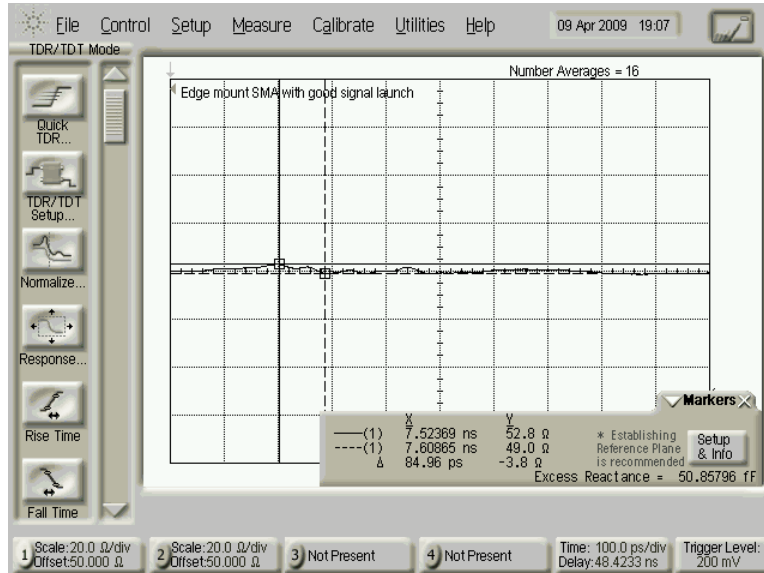


Figure 6. Impedance profile of an edge-mount SMA with good signal launch

Signal Launch Design - Edge-mount BNC

Most connectors have large signal pins of about 25-50 mils diameter. In this case, it is necessary to find a way to avoid the large impedance drop caused by the large landing pad connected to the finer width trace for routing. In this example, the parasitic capacitance of the pad is reduced by removing the metal on the ground and power planes under the pad. This step raises the characteristic impedance of the pad way above 75 Ω (the target impedance for this example). To bring the impedance back to the target of 75 Ω , strips of ground metal are added on both sides of the pad. The ground strips are placed at a pre-determined distance from the pad, such that they introduce just enough ground coupling to achieve the desired impedance¹. This structure has the advantage of being fairly independent from different board stack-ups, and can be re-used in multiple board designs. An alternate implementation is to remove the right size of the metal on the ground and power planes under the pad, such that the fringing capacitance is able to maintain the right characteristic impedance for the pad. Figure 7 illustrates little impedance change from the large landing pad of an edge-mount BNC. Figure 8 shows the top view of the BNC footprint used in this example.

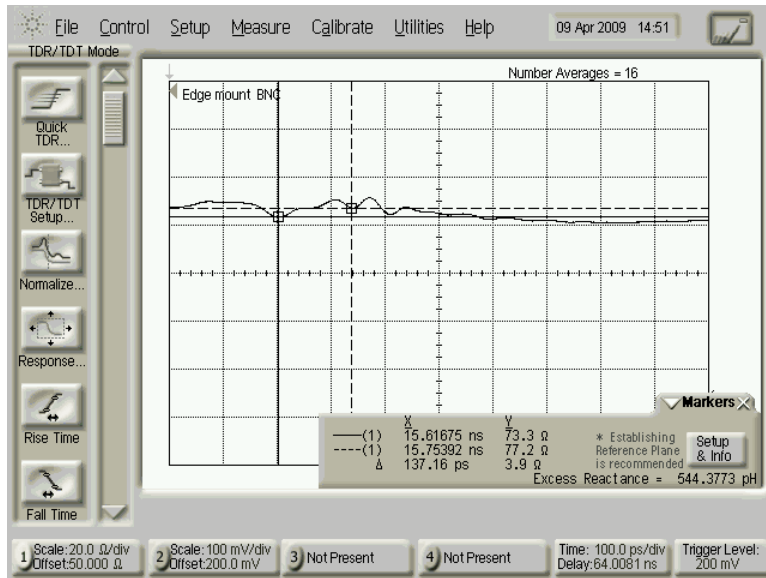


Figure 7. Impedance profile of an edge-mount BNC with good signal launch

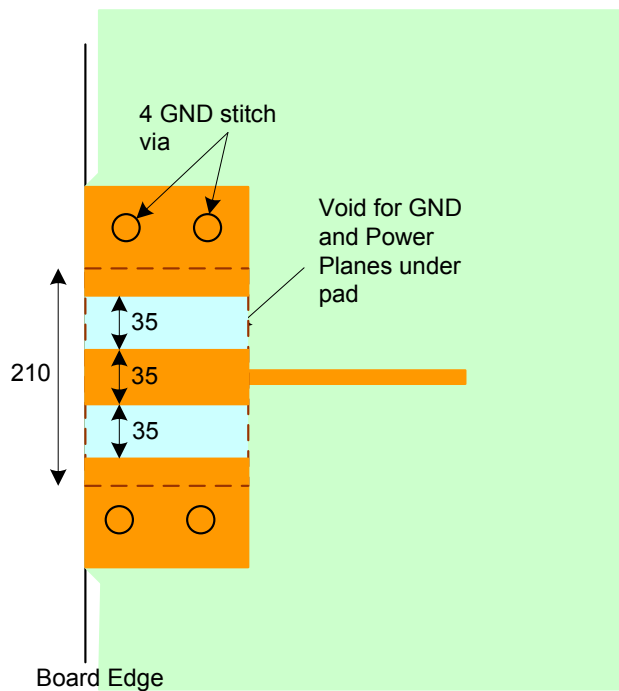


Figure 8. Top view of the edge-mount BNC footprint

Signal Launch Design – Through-hole BNC

For a through-hole BNC connector, the goal is to design a 75Ω controlled impedance through-hole structure. A plated-through hole of 48-mil diameter is used for the signal pin. To achieve the 75Ω impedance for the metal barrel of the hole, a large clearance of about 109 mils from the power and ground planes is necessary. Such a large clearance creates problem for the exit trace from the plated-through hole. The short section of the exit trace within the 109-mil clearance has lost its ground reference and has higher impedance. To solve this problem, a short exit trace with the same width as the donut pad of the hole is used. A strip of ground metal is added on both sides of the exit trace. The ground strips are placed at a pre-determined distance from the exit trace, such that they introduce just enough ground coupling to achieve the desired impedance for the short exit trace¹. This structure consists of a large plated-through hole and its exit trace, both of which are designed to have the same characteristic impedance. This structure has the unique advantage of allowing independent adjustment of the clearance from the planes for controlling the impedance of the hole, and the gap of the ground guards to control the impedance of the exit trace. Figure 9 illustrates little impedance change from the barrel and the exit trace of a through-hole BNC. Figure 10 shows the top view of the BNC footprint used in this example.

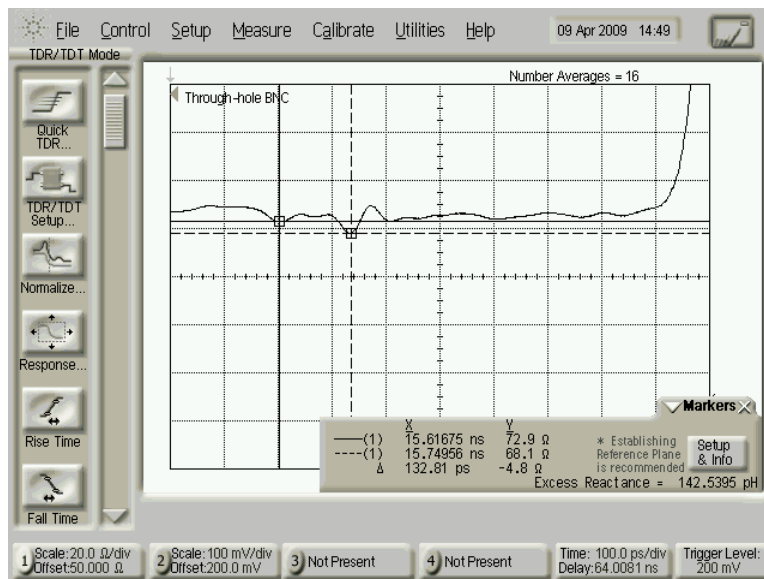


Figure 9. Impedance profile of a through-hole BNC with good signal launch

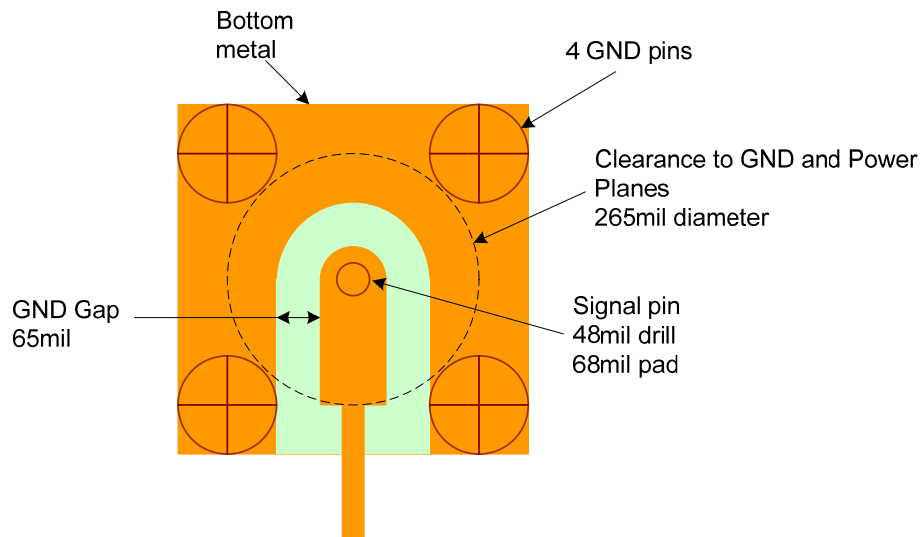


Figure 10. Top view of the through-hole BNC footprint

Conclusion

In this lab report, several common mistakes in signal launch are discussed, and several design examples of improved signal launch footprint designs are presented. The best design is the use of connector with the smallest signal pin, so there is no need to design any special structure. For connectors with larger signal pins, whether it is an edge-mount or a through-hole type, it is possible to design a controlled impedance footprint with a good signal launch. Always use the smallest pad or smallest hole possible. Walk along the signal path, look for the parasitic inductance and capacitance along the path, and find ways to shave off the excess and bring the impedance under control.

While the principles used in this paper apply to signal launch designs, they are also valid for other component landing pads as well. High speed board designs have gone beyond connectivity from point A to point B. There are many subtle layout decisions that have consequences in the electrical performance. Three dimensional electromagnetic simulation tools can aid engineers in making the important layout decisions and achieving the target electrical behavior. The time domain reflectometer is a useful instrument for board debugging and identifying where the impedance changes occur. Good signal launch is a starting point to achieve good signal quality and meeting return loss requirements along with other circuitry on the board.

Reference

1. United States Patent 6765298: "Substrate pads with reduced impedance mismatch and methods to fabricate substrate pads"
2. LMH0302 Datasheet
3. LMH0384 Datasheet
4. National's SDI Feature Website: www.national.com/sdi