

Frequently Asked Questions

1. Where do I buy SDALTEVK? Does it come with the Cyclone III development kit?

The SDALTEVK daughter card can be bought directly from National's [website](#). The daughter card does not come with the Cyclone III development kit. It must be purchased separately from Altera ([link](#)).

2. Is the FPGA source code included in the SDALTEVK box?

The FPGA IP source code is not included in the SDALTEVK box. The source code for the FPGA can be downloaded (for free) from National's FTP server by following steps outlined in Question 4.

3. What are the contents of the SDALTEVK box?

- SDALTEVK daughter card
- End User License Agreement (EULA)
- User Guide (Version 0.5)
- National Semiconductor Broadcast Video Selection Guide
- Schematics of the daughter card
- Bill of materials (BOM)
- Errata (if applicable)

4. How do I get access to the source code for Altera Cyclone III FPGA IP?

To get access to the source code for the Altera Cyclone III FPGA,

- The customer has to download the SLA (Software License Agreement). The form can be downloaded from National's [website](#).
- The customer has to fill and sign the form.
- The completed form can be scanned and sent as e-mail or faxed to the local National representative. The customer also needs to provide their mailing address as a part of the SLA.
- Once National receives the SLA, it will be processed. The customer will receive a login ID and password to National's FTP server that hosts the FPGA code.
- The customer can use this login to download the FPGA IP source code.

5. What formats are the source code available in?

The source code is available in both Verilog and VHDL formats. The user must log into the FTP download site and follow the "Smart SerDes Downloads" link to the Downloads page. In the Downloads page, both the Verilog and the Vhdl versions of the source code are compressed into a single Zip file:

Triple Rate - Altera FPGA IP v-1.5 Dec 2008.zip

The user can uncompress the zip file using Winzip or similar software to access the individual module files. The Vhdl files have an extension **".vhd"** and the verilog files have an extension **".v"**

6. What is the latest version of the code? Will I get notification of any source code updates?

In the Downloads page, the file **Latest Release.txt** contains information on the latest release version. There are no automatic notifications for code updates. Customers must check regularly for updates.

7. What is the directory structure of the source code?

To view the source code of the FPGA, the user must download the file Triple Rate - Altera FPGA IP v-1.5 Dec 2008.zip and extract it to a local directory using Winzip or a similar software.

The directory structure after extraction:

Altera\DOCS: This directory has the Firmware description document and the Release notes.

Altera\CONTROL_ALTERA: In order to provide a user interface and to control the I2C devices a microcontroller system is implemented in the firmware. This is based around the ZPU core available from www.opencores.org. This is attached via wishbone bus to various sub-modules: An I2C interface, serial UART and Debug port (which provides access to switches and LEDs on the motherboard). There is an interface module between the wishbone bus and the registers in the video firmware. This directory contains the modules that implement the Zpu core and control interface.

Altera\RTL_VERILOG_ALTERA: This directory contains the source code in Verilog format.

Altera\RTL_VHDL_ALTERA: This directory contains the source code in VHDL format.

Altera\SOFTWARE: This directory contains the source code in VHDL format.

Altera\SYNTH: This directory contains the source code in VHDL format.

Altera\TESTBENCH: This directory contains the source code in VHDL format.

8. Where do I locate information about the FPGA IP? Where is the FPGA IP description document located?

The Firmware description document is located in Altera\DOCS directory. The document provides a detailed description of the various modules and modes supported by the FPGA IP.

9. What are the formats supported the FPGA IP?

	Format	Specification
SD	576i25	SMPTE 259M /C
	486i29	SMPTE 259M /C
HD	720p23	SMPTE 292M
	720p24	SMPTE 292M
	720p29	SMPTE 292M
	720p30	SMPTE 292M

	720p50	SMPTE 296M
	720p59	SMPTE 296M
	720p60	SMPTE 296M
	1080sf23	SMPTE 274M + RP211
	1080sf24	SMPTE 274M + RP211
	1080i25	SMPTE 274M
	1080i29	SMPTE 274M
	1080i30	SMPTE 274M
	1080p23	SMPTE 274M
	1080p24	SMPTE 274M
	1080p25	SMPTE 274M
	1080p29	SMPTE 274M
	1080p30	SMPTE 274M
3G	1080p50	SMPTE 424M
	1080p59	SMPTE 424M
	1080p60	SMPTE 424M

10. Is Dual link supported in this FPGA IP?

At this time, Dual link formats are not supported for Cyclone III FPGA. National provides FPGA source code for Dual link formats for other vendors' FPGA. The source code conversion from one FPGA must be done by the user.

11. What are the audio formats supported by this FPGA IP?

Currently the FPGA source code supports 4 simultaneous channels of audio embedding/de-embedding. The 4 channels can be chosen from one of 4 groups. The audio format supported is I2S. Audio support for AES formats will be added shortly.

12. Who do I contact for support?

For any issues related to the FPGA IP, please contact your local National Semiconductor representative.

13. Are there other sources of FPGA IP source code?

Yes. Altera provides its own source code for SMPTE protocol processing on Cyclone III FPGAs. Customers can download the source code from Altera's [FTP site](#). Customers must note that National does not support any issues related to Altera's source code and that the customers must contact Altera directly for any support.