

## Setup and Operating Instructions — SD131ASM Rev. F, Command Rev. 1.0

### **READ COMPLETELY BEFORE ATTEMPTING TO USE THIS EQUIPMENT.**

#### **SD131ASM Specifications —**

**DC input power:** 7.5Vdc to 9.0Vdc  $\pm 5\%$  @ 500mA, HD rate (except when programming the COP8 uC). Power supply ramp-up time <4ms. All device supplies are regulated on-card.

**Operating temperature range:** +10°C to +30°C (limited by crystal or oscillator module)

**RS-232 Command port:** RS-232 standard levels for input and output. 9600 baud, 8 data bits, 1 stop bit, odd parity, no flow control. Set the terminal or terminal emulator program to append a line feed after received carriage return characters. Turn off local echo on terminal or terminal emulator program (The “Hyperterminal” program is recommended).

**Serial Data Inputs:** SMPTE 259M or SMPTE 292M standard levels and impedances. Inputs are not equalized for cable losses or fully compensated for return loss.

**Parallel Video Data and Other Inputs and Outputs:** See LMH0031 datasheet for output port drive levels and other specifications. The SD131ASM has provision for user installed connectors at all CMOS inputs and outputs.

#### **SD131ASM Preliminary Setup —**

##### **Jumper Settings: (Refer to assembly drawing for jumper settings.)**

**JP1** (uC & RS-232 port power): This jumper must be set to 5V for all SD131ASM assemblies.

**JP3** (DCE/DTE): Set this jumper pair to configure the RS-232 port for either Data Communications Equipment (DCE), the normal mode when communicating with a PC serial port, or Data Terminal Equipment (DTE) for other types of computer equipment or specific applications as required. To set the communications mode, the jumpers are aligned in the same direction as the legend for the type of connection required, i.e. both jumpers align parallel with the legend DCE (default) or with DTE (optional).

**JP4: Do not use or connect to external devices.** Improper operation may result.

##### **DC Power Supply and Wiring—**

**It is strongly recommended that the power supply used to power this assembly have both voltage and current limit setting capability. It should also have a DC output ON/OFF switch and DC output metering. A supply such as the Agilent E3632A meets these requirements.**

Attach suitable gauge wiring (#18 or 16AWG suggested) and connectors for supplying the regulated 7.5V to 9.0V $\pm 5\%$  main power to the SD131ASM. Use of 0.25” crimp-on spade type receptacle terminals is recommended. A crowbar diode is provided to reduce possible damage to the SD131ASM in the event that main supply polarity is reversed when connecting the SD131ASM to the power supply. In addition, the automotive-type regulators used in this design provide additional fault protection. **It is suggested that the power supply current limiting be set to 1A.**

##### **BIST and TPG Operation—**

The Built-In Self-Test (BIST) capability of the LMH0031 may be used to partially test the SD131ASM. The SD131ASM may also be used as a Test Pattern Generator (TPG) having parallel test data outputs. When using BIST or TPG mode, control register 0Dh must be loaded with the code for the test pattern desired and the TPG Enable bit must be set. Instructions for accessing the BIST and TPG modes of the LMH0031 are described in the device datasheet.

**RS-232 Command Port Communications —**

The SD131ASM is supplied with the RS-232 port configured to operate with standard IBM-PC/AT 9-pin serial ports. PC serial ports are configured as DTE. The SD131ASM is therefore configured as DCE (like a modem, for example). A suitable 9-pin serial port extension or modem cable may be used to connect the SD131ASM to the PC. Other control devices such as dumb terminals may also be used to communicate with the SD131ASM. Consult the equipment manual for the required communication settings as DTE or DCE. Dumb terminals are commonly DTE.

The port uses RS-232 standard levels for input and output. 9600 baud, 8 data bits, 1 stop bit, odd parity, no flow control. Set the terminal or terminal emulator program to append a line feed after received carriage return characters. Turn off local echo on terminal or terminal emulator program (The “Hyperterminal” program is recommended).

**Serial Data Inputs —**

The SD131ASM serial data inputs (SDI) may be connected to external test generators or other equipment using suitable 75 $\Omega$  coaxial cables. Characteristics of signals and maximum input levels supplied to the SDI shall comply with either SMPTE 259M or SMPTE 292M. The SDI are DC terminated in 75 $\Omega$  and are AC-coupled to the device inputs. The SD131ASM does not employ a cable equalizer; therefore, cables connecting signal sources to the SDI should be restricted to less than 1 meter total length for best signal fidelity and preservation of signal risetimes.

**Parallel Video, Clock, Ancillary/Control Data and User Bus Inputs and Outputs —**

Double-row pin (or socket) connectors may be installed at positions provided for P1 through P4. Connectors may be installed either on the top or bottom side of the SD131ASM. These connectors together with suitable cabling provide access to all necessary data inputs and outputs of the LMH0031. Consult the LMH0031 datasheet for electrical and loading requirements of these inputs and outputs. Cable lengths should be as short as possible to minimize signal degradation due to reflections and noise. Each input terminal is paired with a ground terminal. When ribbon or similar cable is used to carry signals to or from the SD131ASM, signal conductors are automatically paired with a ground conductor. Due to the wide variation of possible cabling schemes that may be used with the SD131ASM, termination resistors are not installed. It is recommended that series termination of the proper value for the cable impedance used be employed at the source end of the cable supplying signals to the SD131ASM. For example: The series termination value for ribbon cable is 100 to 120 $\Omega$ . The series termination for 50 $\Omega$  coaxial cable is 47 to 51 $\Omega$ . For 75 $\Omega$  coax, the value is 75 $\Omega$ .

**NOTE:** P4 serves as both the control port and ancillary data port connection. The COP8 controller places its outputs in tri-state when not communicating with the LMH0031. External equipment used to interface to the Ancillary/Control Data port must have tri-state-capable outputs. The outputs must be placed in tri-state when not driving these lines. Otherwise, conflict with the COP8 outputs will result when it attempts to communicate with the LMH0031. Conversely, attempts to access control information in the LMH0031 should not be made while using the port to output ancillary data.

**SD131ASM Command Summary (Rev. 0.9)—**

At reset or power-up, the COP8 toggles ACLK 3 times. This insures a proper reset of the LMH0031 Ancillary/Control port (see device datasheet for details). After a command is executed, the COP8 tri-states the AD[9:0], ACLK, RD/WR(bar), ANC/CTRL(bar) lines. This allows other equipment to transmit or receive signals from these inputs and outputs.

**NOTE:** The outputs of external equipment used to drive the control port must be placed in tri-state when not driving the port. Otherwise, conflict with the COP8 outputs will result when it attempts communication with the LMH0031 control port.

**Valid Control Commands —**

The following commands are used with the LMH0031: Commands are case-sensitive and should be upper case only.

**W** when received, starts the control register write sequence.

**R** when received, starts the control register read sequence.

**P** when received, continuously repeats the control register read sequence of the address last entered.

**K** when received, toggles ACLK once.

**L** when received, clears all control registers (all writeable bits).

**M** when received, displays the contents of all LMH0031 registers on the terminal.

**T** when received, begins extraction of all words from the ancillary data FIFO.

**X** when received, extracts one word from the ancillary data FIFO.

**Z** when received, starts CRC error polling.

**%** when preceding the next eight 0 or 1 characters indicates binary data follows. Used with the **W** command.

**Unused Commands**

The following command appears on the terminal display but is used only with the LMH0030:

**I** – LMH0030 ANC FIFO insert command.

**W – Write to LMH0031 control registers**

After entering **W**, the next 2 valid characters entered are taken as the write address in hexadecimal. The next 2 valid characters entered are taken as the write data in hexadecimal. No termination (CR/LF) is needed. Entry of the last valid data character initiates the write sequence.

Example: The character sequence **W0B43** writes 43h to register 0Bh.

If a **%** character is received, the next eight 1 or 0 characters are taken as binary data to be written. No termination (CR/LF) is needed. The eighth valid character initiates the write sequence.

Example: The character sequence **W0B%01000011** writes 01000011b (43h) to register 0Bh.

Once the write mode is entered, the COP8 stays in write mode until ‘Enter’ or a **R**, **X**, **M** or **L** character is received. Additional register addresses and data may be entered separated by the ‘space’ character. Therefore, a sequence such as: **W141B 151C 161D** is valid and writes 1Bh to register 14h, 1Ch to register 15h and 1Dh to register 16h.

‘Enter’ terminates and exits the write command sequence.

**R – Read from LMH0031 control registers**

After entering **R**, the next 2 valid characters entered are taken as the read address in hexadecimal. No termination (CR/LF) is needed. The second valid character entered initiates the read sequence. The COP8 responds with the hex value and binary value read from the register addressed followed by a CR/LF character.

Once the read mode is entered, the COP8 stays in read mode until ‘Enter’ or a **W**, **X**, **M** or **L** character is received.

Example: The sequence: **R14 15 16** is valid and reads from registers 14h, 15h and 16h. In this case, the COP8 responds with the sequence:

R14 1B 00011011

15 1C 00011100

16 1D 00011101

‘Enter’ terminates and exits the read command sequence.

**P – Continuously rePeat reading from the last LMH0031 control register address entered**

Following P, a read operation to the last control register address entered is continuously repeated. The results of the read operations are sent to the terminal. This command is useful when monitoring dynamically updated registers and bits like the H-V-F bits, CRC error registers or the format register.

**T – ExTract all words from the ANC data FIFO**

After entering T, and with the ancillary data FIFO clock properly enabled, all words are extracted from the FIFO to the ancillary/control data port. Refer to instructions on the K command before using this command.

**X –EXtract one word from the ANC data FIFO**

After entering X, and with the ancillary data FIFO clock properly enabled, one word is extracted from the FIFO to the ancillary/control data port. Refer to instructions on the K command before using this command.

**M – Display all LMH0031 control registers**

This command displays the contents of all primary control register on the terminal.

**K – Toggle ACLK once**

This command is used when enabling the ancillary data FIFO to output data using either the T or X commands. The distribution of the ancillary clock to the FIFO is initially disabled at power-on or after the part is reset. This is done to reduce power supply current unless ancillary data operations are required. To enable the ancillary clock so that the data may be extracted from the FIFO, the FIFO CLOCK ENABLE (bit 6 of ANC5, register 17h) must be set and Aclk must then be toggled three (3) times to propagate the command to the FIFO control logic.

**L – Clear all LMH0031 control registers**

**Use with caution!** Clears all writeable bits in all control registers.

**Z – Enable CRC error polling**

This command begins a routine which polls for CRC errors. This is useful for monitoring for errors in received data.

**Document Revision Status: SD131ASM\_OPINST**

Rev. 0.0 — Initial document release, 22 March 2002.

Rev. 0.1 — Corrected command summary, 28 March 2002.

Rev. 0.2 — Revised to support Rev. E PCB release, 23 Sept. 2002.