

# CLC001, LMH0002 (CLC002), CLC007, CLC011, CLC012, CLC014, CLC016, CLC020, CLC021 - Frequently Asked Questions (FAQs)

National Semiconductor



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## What should be done with the unused output of the LMH0002 (CLC002)?

The unused output of the LMH0002 (CLC002) should be terminated with 75Ω to ground. The entire network for the unused output should consist of the standard 75Ω pullup to V<sub>CC</sub>, followed by a series 1μF capacitor, followed by the 75Ω termination to ground.

**Relevant Part:** CLC002; LMH0002

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## Can the CLC012 or CLC014 equalize Alternate Mark Inversion (AMI) coded data?

No. Alternate Mark Inversion (AMI) is a tri-voltage level data coding method whereby a space is represented by 0 Volts and successive marks by alternating positive and negative voltages with respect to 0V. The objective is to produce a net 0 Volt DC residual (common mode) offset.

The CLC012 and CLC014 adaptive cable equalizers cannot process such tri-level voltage coded signal standards. The CLC012 and CLC014 are designed to process bi-voltage level coded, AC-coupled signals with fundamental ECL-like characteristics (800mV +/-10% Pk-Pk, 1ns +/- 0.5ns risetimes).

**Relevant Part:** CLC012; CLC014

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## What are pathological signals? How can they affect equalizer (CLC014) and PLL (CLC016) performance?

Pathological signals are specific patterns of low transition density that stress SDI receivers. These signals are a side effect of the scrambler used in SDI systems.

A pathological signal that stresses the cable equalizer consists of 19 bits of one polarity followed by 1 bit of the opposite polarity. The PLL section of the receiver is stressed by a pathological signal that consists of 20 bits of one polarity followed by 20 bits of the opposite polarity. A third pathological signal that usually doesn't cause problems consists of a series of 44 bits with no transitions (or 59 transition-less bits for HD). Pathological signals are covered in detail in SMPTE EG34.

The equalizer and PLL pathological signals are combined to form the SDI Checkfield, with the top half of the frame being the equalizer pathological and the bottom half of the frame made up of the PLL pathological. SMPTE RP178 and SMPTE RP198 document the SDI Checkfield for SMPTE 259M and SMPE 292M, respectively.

National's Broadcast Video products are fully tested with pathological signals. The CLC016 is designed not to lose lock during pathological conditions. The CLC014 is insensitive to pathological signals as long as its input coupling capacitor is sufficiently large.

**Relevant Part:** CLC014; CLC012; CLC016

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### Can the CLC016 reclock DVB-ASI data?

The answer to whether the CLC016 can reclock DVB-ASI data is not as simple as it may at first appear. DVB-ASI (Digital Video Broadcast-Asynchronous Serial Interface) is a compressed data transmission standard that can carry MPEG2 compressed video and many other types of data over a common network. It has a nominal transport data rate of 270Mb/s but the effective payload data rate can vary widely from a few kb/s to about 200Mb/s. The transport stream's signal characteristics differ markedly from SMPTE 259M serial digital video (SDV). The DVB-ASI serial data stream is characterized by high harmonic content and often by high dependent jitter. These are products of the coding and clocking processes used in the DVB equipment. The virtually infinite variation in data payload and content and the signal characteristics present uncharted difficulties for receivers and reclockers designed for standard SDV.

The CLC016 uses a Hogge phase detector which is designed to handle the pathological data content specific to SDV. The CLC016 is also designed to resist locking to harmonics of the data transport rate. When operating in Auto-Rate Mode (ARM), the harmonics present in the DVB-ASI signal can cause conditions which drive the PLL out of the phase range over which it can maintain lock. When this is combined with data jitter, the CLC016 can be driven to lose lock. It will then go into its rate hunting mode in an attempt to re-lock to the incoming data.

The CLC016 can be made more robust when it must handle DVB-ASI data by operating it in Manual Rate Mode and selecting the 270Mb/s rate; or the reclocker circuit may be designed for single frequency operation. Single frequency operation uses only one rate resistor to set the VCO frequency to 270Mb/s. One terminal of that resistor is connected to the RTN input and the other terminal to inputs R0 through R3 connected in parallel. In a single frequency design, ARM may be used.

If ARM is used in a multi-data rate system which must handle DVB-ASI data, and locking in the presence of data jitter is a problem, then increasing the loop bandwidth by increasing the  $R_{BW}$  resistor in the loop filter should make the CLC016 better able to track the instantaneous input frequency changes but at the expense of increased output residual jitter.

**Relevant Part:** CLC016

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### How do you configure the CLC016 to lock to a single, specific data rate?

Use the equation in the datasheet to calculate the appropriate rate setting resistor value. The equation is as follows:

$((1000\text{Mbps} / f_{\text{CLK}}) - 0.2) * 1\text{k}\Omega$ , where  $f_{\text{CLK}}$  is the desired data rate.

Select the nearest 1% resistor value and use this value in place of one of the four rate setting resistors. For the SD901EVK, this would be R11, R12, R13, or R14. The CLC016 should automatically select the correct rate setting resistor when you apply the corresponding data rate at the input. If this is the only data rate you are interesting in locking to (or if you are having problems locking to the wrong data rate), you can do one of three things:

1. Tie the other 3 rate setting resistors together (short R12, R13, and R14 on the SD901EVK with 0- $\Omega$  resistors),
2. Replace all four rate setting resistors with your calculated resistor value.
3. Configure the CLC016 for manual rate mode and manually select the data rate with RD0 and RD1.

To configure manual rate mode, you must set the AUTO line low (set the AUTO jumper in JP3 of the SD901EVK) and short the CARS capacitor to VEE (set the jumper in JP4 of the SD901EVK). You then manually select the data rate with the 2-bit bus consisting of RD0 and RD1. To select the R0 datarate (R11 on the SD901EVK) you set both the RD0 and RD1 jumpers in JP3, which pulls them both to ground. Refer to the [SD901 User Guide](#) for more details:

Note that the four rate setting resistors must either be stuffed or tied together; you should not leave any of the rate setting resistors open. If one the resistors is left unconnected while in auto rate mode the CLC016 can get "stuck" as it cycles through the resistors looking for a lock.

**Relevant Part:** CLC016

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### **For the CLC020: How can the value of Rref be determined to give output levels other than 800mV? What is the approximate min-max output level range?**

The output level swing of the CLC020 and CLC021-5V are controlled by an external resistor,  $R_{REF}$ . The output is designed to produce a level swing of 800mVp-p (10%) with a resistor value of 1690  $\Omega$ . The standard output load is 75  $\Omega$  DC (to ground) and an AC-coupled 75  $\Omega$  coaxial cable and termination. The output level is inversely proportional to the value of  $R_{REF}$ . A useful approximation to find  $V_{out}$  for other values of  $R_{REF}$  is:  $V_{out}(mV) @ (1800 - 0.767 \times R_{REF} + 1.052 \times 10^{-4} \times R_{REF}^2)$ . The useable range of this approximation is from about 1.5k to 3.6k  $\Omega$  for output levels from about 900 to 375mVp-p.

**Relevant Part:** CLC020; CLC021-5V

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### **What should be done about the unused output of the CLC001, CLC020, or CLC021?**

You should terminate the unused output to ensure a balanced output drive. In the typical application circuit, the output sees 75 $\Omega$  DC-wise and 37.5 $\Omega$  AC-wise (during transitions). Use a 75 $\Omega$  pulldown on the unused output to meet the DC condition

**Relevant Part:** CLC001; CLC020; CLC021

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### **Why do the CLC001's outputs toggle when no input signal is applied and the inputs are biased to the same DC level?**

The input buffer of the CLC001 is comprised of both P-channel and N-channel differential amplifiers connected and operating in parallel. This topology achieves the rail-to-rail common mode voltage specification. The actual input sensitivity (i.e. gain) is higher than the data sheet would seem to indicate. When the input differential voltage is nearly zero the amplifier's gain is a maximum. Thus, any small input signal such as noise will cause the amplifier to toggle randomly or oscillate. The data sheet sensitivity figure is conservative and it includes such factors as tester guard band. It is intended to provide designers a safe minimum figure.

In cases where the inputs may be unconnected or be AC coupled, the input bias circuit should provide a small offset voltage between the inputs. An input bias circuit that provides a differential offset of about 12 mV to 24 mV should keep the device from toggling. The added voltage offset should not cause any significant duty cycle distortion.

**Relevant Part:** CLC001

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#### **Can the CLC001 act as a level translator, such as in converting LVDS to LVPECL?**

No. The CLC001 is a cable driver and not a level translator. The CLC001 output cannot DC connect to LVPECL inputs. It must be AC coupled into any ECL device input since it is ground referenced and ECL is positive supply referenced.

The CLC001 has a wide input range, accepting both LVPECL and LVDS input swings. Its outputs produce an "LVPECL-like" output. Its outputs are optimized for driving cable in an AC coupled environment. As such, it is inappropriate as a level translator.

**Relevant Part:** CLC001

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#### **Can the output of the CLC001 drive 50Ω loads?**

The CLC001 can drive 50Ω loads, but the peak to peak output swing will be reduced. It is stated in the datasheet that the CLC001 is designed for 75Ω AC loads, and not intended for 50Ω. The CLC001 is only capable of driving up to 667mV into 50Ω.

**Relevant Part:** CLC001

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#### **Can the CLC007 replace the Gennum GS9007? What circuit, component and PCB changes are needed?**

Except for the inputs, the application circuit for both devices is similar. Here are the steps to replace the GS9007 with the CLC007.

1. The existing PCB layout most likely can be used as is. The CLC007 has the same footprint as the GS9007. The main difference is input coupling.
2. The GS9007 has internal input coupling capacitors. The input of the CLC007 does not have these capacitors. This may or may not present a problem depending on the device feeding the CLC007. Both devices must be powered from the same supply voltage or have a common Vcc connection. If the device preceding the CLC007 has an output voltage swing from Vcc-0.8V to Vcc-2.5V, the coupling capacitors are not needed. The CLC007 can be DC coupled to the device without additional components. The PCB layout is unaffected. However, if the output voltage swings to Vcc or below Vcc/2, a coupling capacitor and bias resistors are needed to couple the CLC007 input(s). This may require a PCB layout change for the additional components.
3. The GS9007 has ECL outputs and uses output pull-down resistors. Remove these resistors from the PCB. They are not needed with the CLC007.
4. The output matching network(s) for the GS9007 may use a 1.8pF caps across the 68 Ω series output matching resistor(s). Generally these are not required for the CLC007 and may be removed.

**Relevant Part:** CLC007

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### **How does the CLC011 detect End of Active Video (EAV)?**

End of Active Video (EAV) determines the start of the horizontal blanking interval in digital video. EAV is identified in the data stream by the Timing Reference Signal (TRS) consisting of the words: 3FF, 000, 000, XYZ. The CLC011 decodes the fourth word of the TRS (the XYZ word) to detect EAV. The decoding is explained in Tables 3 and 4 of SMPTE 125M.

When EAV is detected with component video, the CLC011's EAV (pin 1) is logic low for one cycle of the parallel clock. For composite video, EAV is always asserted high.

**Relevant Part:** CLC011

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### **How does one apply proper framing while using the CLC011 with non-SMPTE data?**

In the SMPTE application for which this device was designed, the pattern 3FFh, 000h, 000h is used at the start and end of each video line as a Timing Reference Signal (TRS). The CLC011 uses this pattern to determine the framing (where to place the word boundaries). If this pattern is seen in a non-SMPTE application, the CLC011 will readjust its framing and the received words will be shifted.

In a non-SMPTE application, an initialization pattern of 3FFh, 000h, 000h should be sent to sync up the CLC011. Then the FE (Frame Enable) input on the CLC011 should be taken to a low state, which will prevent it from realigning the word boundary if it sees this pattern again in the data being transmitted.

**Relevant Part:** CLC011

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### **How does the CLC011 handle TRS characters that do not comply with SMPTE 259M?**

The CLC011 will not recognize TRS character sequences that do not comply fully with the SMPTE standard. The CLC011 requires a valid SMPTE 259M TRS sequence of 3FFh, 000h, 000h. The CLC011 compares the entire 30 bit sequence as it is decoded. If the 30 bits are not 3FFh, 000h, 000h, then no TRS is detected.

**Relevant Part:** CLC011

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### **When the CLC014 or CLC012 equalizer is used to drive the DDIs of the CLC016 retimer, must I use the diode or resistor dropping network between the equalizer's output load resistors and Vcc?**

No. The CLC016's input common mode range extends to Vcc. The outputs of the equalizer will need only the pull-up load resistors to Vcc. Locate these load resistors at the inputs of the CLC016 or as the last component at the receiving end of the network.

**Relevant Part:** CLC012; CLC014; CLC016

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### **Can both outputs of the CLC012, CLC014, or CLC016 be forced either high or low? What states do the outputs go to when MUTE is applied?**

The outputs of the CLC012, CLC014, or CLC016 are never both high or both low. You can't latch the outputs to a particular state due to the differential output design. One output is always high, and the other is always low (800mV less). In other words, one output transistor will always be "on" and sinking current, while the other is off, so the outputs will always be at opposite states. When you MUTE the outputs, they behave the same as if no input is connected, with one output high and the other low. Once the input is removed or muted, the outputs will remain in their present high or low state until a transition is detected.

**Relevant Part:** CLC012; CLC014; CLC016

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### **What is the purpose of having the R-C network in the unused input of the CLC014 or CLC012?**

The purpose of the series R-C network in the unused input is to cause the common-mode noise cancelling properties of the differential input stage to reject RFI and other common-mode signals that may be induced into the input networks. Without equal impedances in both inputs there would be a net differential mode gain resulting from the different currents flowing in the input networks.

**Relevant Part:** CLC012; CLC014

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### **Can the CLC014 or CLC012 equalize tri-level or other multi-level voltage coded data signals?**

No. The CLC014 and CLC012 cable equalizers are designed to equalize only AC-coupled, bi-level coded digital data signals having a nominal transmitted level of 800mVp-p,  $\pm 10\%$ . This class of signal includes NRZ, NRZI, Bi-phase Mark, Bi-phase Space, etc.

**Relevant Part:** CLC012; CLC014

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### **In the unused input of the CLC014 (or CLC012), can I use a single 137 $\Omega$ resistor in place of the series connected 100 $\Omega$ and 37.4 $\Omega$ resistors in the R-C network?**

Yes. A single 137  $\Omega$  resistor may be used.

**Relevant Part:** CLC012; CLC014

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### **Can cable clones be used to test the CLC014 or CLC012?**

No, all testing must be done using real coaxial cable of the kind recommended in the data sheet. The devices are production tested using Belden 8281. The attenuation vs. frequency characteristic of cable clones can differ significantly from that of coaxial cable. Cable clones do not have the monotonic, near-infinite stop-band attenuation as does the equivalent length of coaxial cable. Therefore, the output contains excessive residual high frequency energy. Since the CLC014 and CLC012 use the high frequency energy of the input signal to determine how much equalization to apply, the use of cable clones can cause the CLC014 and CLC012 to exhibit false under-equalization of the signal.

**Relevant Part:** CLC012; CLC014

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### **Can the CLC014 or CLC012 be used with transformer input coupling?**

No. The CLC014 and CLC012 are not designed for transformer coupling. The device is specifically designed for capacitor coupling according to SMPTE 259M. Transformer coupling alters the frequency spectrum of the signal. It does not preserve the low frequency energy content and distorts the high frequency content. This causes the CLC014 to under-equalize and may cause other unpredictable effects.

**Relevant Part:** CLC012; CLC014

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### **Why are pathological patterns causing problems for the CLC012 or CLC014?**

The coupling capacitors may be too small. A value of 1  $\mu\text{F}$  or higher is necessary to handle the large DC shifts and transition-less intervals present in serial digital video data. Use only high quality RF ceramic capacitors for coupling capacitors.

**Relevant Part:** CLC012; CLC014

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### **How does one connect the output of the CLC014, CLC012, or CLC016 to an LVPECL input?**

Connecting the output of the 5V CLC014, CLC012, or CLC016, which all have open collector outputs, to a 3.3V LVPECL input presents a number of issues. The main point to consider is that the CLC014, CLC012, and CLC016 have a minimum supply voltage requirement on DO of  $V_{CC} - 1.6\text{V}$  (See the Recommended Operating Conditions in the respective datasheet). The reason being is that the emitters of the output transistors are clamped at about  $V_{CC}/2$ , so the output transistors are cut off if you attempt to operate them at a lower DC bias. Three possible solutions are explored:

1. AC coupling.

This is the simplest solution, although it is not always possible with all applications.

2. Resistor divider network.

There are several problems with using a resistor divider network to shift this voltage down. Since the CLC014/012/016 output is a current sink tied to +5V, any resistive load you put on it to ground will create a standing load current. If you make the standing current small, the resistors from the CLC014/012/016 to ground will be large, and this causes frequency problems. If you make the standing current large, more power is burned in the loads. Either way, the standing current will present problems for the output transistor. Its operating point will shift due to the new voltage, and the transistor won't sink its normal current.

3. Dedicated PECL to LVPECL translator.

A PECL to LVPECL translator may be used, such as ON Semiconductor's MC100LVEL92.

**Relevant Part:** CLC014; CLC012; CLC016

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### **For the CLC014, does the $C_{AEC}$ capacitor value depend on the type of cable being used? Is the R value in the datasheet table page 10 different for coaxial or twisted pair cables?**

The R parameter given in the table on page 10 of the [CLC014 Datasheet](#) depends on cable length not cable type. The R values given are valid for any cable having a normal attenuation versus frequency characteristic. The cable can be either coaxial or twisted pair. The R value is essentially the current source (equivalent) resistance supplying the  $C_{AEC}$  cap from the integrator. It determines

the charge time of the integrator and hence the response time of the device to a change in cable length. Since the cable length will most likely remain constant after a piece of equipment is installed, the capacitor value should be set for the most common (or average) length of cable.

**Relevant Part:** CLC014; CLC012

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#### **Can the CLC016 lock to CMI data?**

Yes. CMI encoded data has transitions on both the rising and falling edge of the clock, so it looks like the data rate is twice that of an NRZ encoded signal. Therefore, when using the CLC016 for 155 Mbps CMI encoded data, it should be set up as if the data rate were 311 Mbps.

**Relevant Part:** CLC016

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#### **What are the tradeoffs for the CLC016's loop filter bandwidth?**

Narrower bandwidth makes it more difficult for the CLC016 to lock to signals but results in lower residual jitter. Wider bandwidth improves acquisition time and jitter tolerance but increases residual jitter.

**Relevant Part:** CLC016

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#### **When using the CLC016 at a single frequency, what should be done with the other frequency setting resistor inputs?**

Tie them all together to the single resistor. This will prevent the possibility of selecting an unused frequency setting resistor input and thus placing the device in an unrecoverable condition.

**Relevant Part:** CLC016

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#### **Can the parallel clock be applied before the CLC020 or CLC021 is powered up?**

No, unless the manual reset is used (CLC021 only). In the case of the CLC020, the parallel clock, PCLK, should not be asserted until at least 30 m s after power-on. The same is true for the CLC021, unless the manual reset is used. If manual reset is used during power-on, then PCLK may be asserted at any time as long as manual reset is not de-asserted until the part is fully powered.

**Relevant Part:** CLC020; CLC021

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#### **Is the CLC002 and the LMH0002 the same device?**

Yes, this was a name change only for the CLC002. The new SDI family of parts used the LMH prefix and a four digit number instead of the CLC prefix with three numbers.

**Relevant Part:** CLC002; LMH0002

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