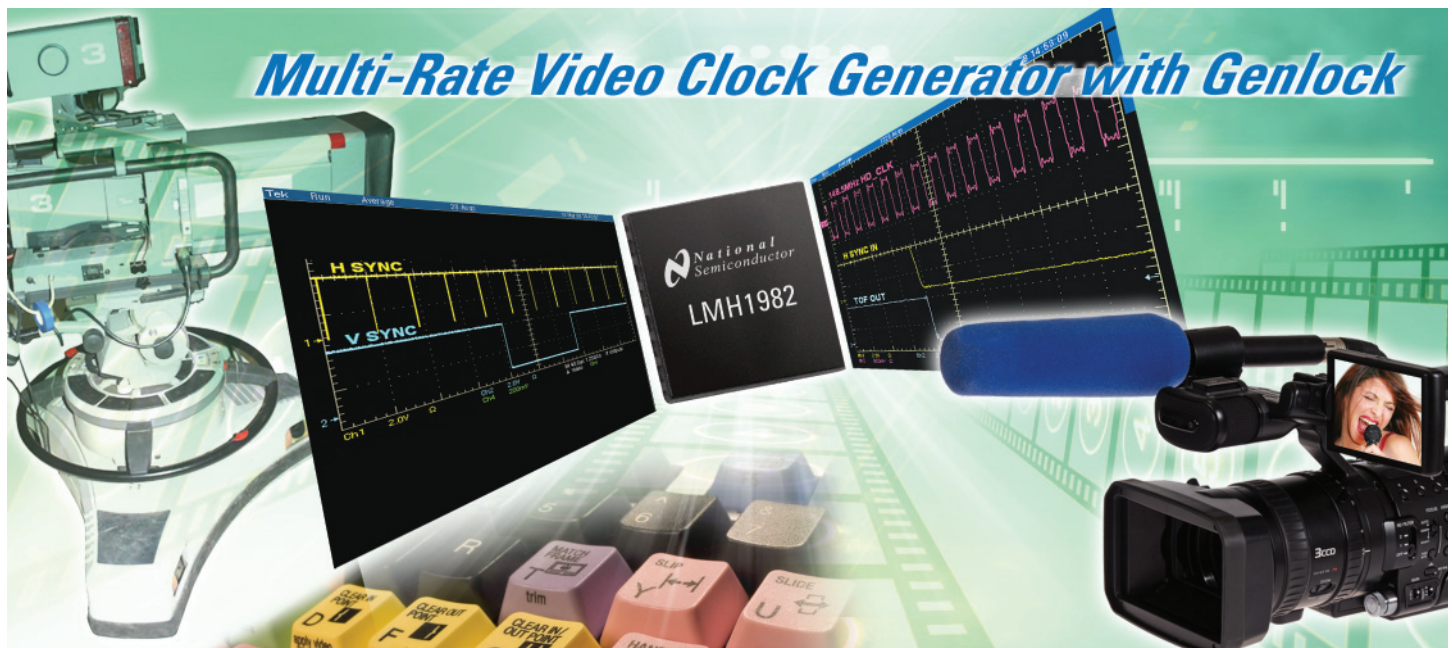


# Industry's Lowest-Jitter Integrated Multi-Rate 3G/HD/SD Clock Generator with Genlock



## Introduction

The LMH1982 is a multi-rate video clock generator ideal for use in a wide range of applications including video genlock, SDI Serializer and Deserializer (SerDes), video capture, video conversion, video editing, video displays, and other broadcast and professional video systems.

The LMH1982 can generate two simultaneous SD and HD output clocks and an output Top of Frame (TOF) timing pulse. Only one external 27 MHz VCXO is required to operate the LMH1982. The low-jitter output clocks are capable of directly driving FPGA serializers with no additional clock cleansing required. In genlock mode, these output signals can be phase locked to H and V sync signals applied to either of the two reference ports. The input sync signals can come from an LMH1981 video sync separator or an FPGA SDI deserializer. When a loss of reference occurs, the device can be configured to default to either free run or holdover operation.

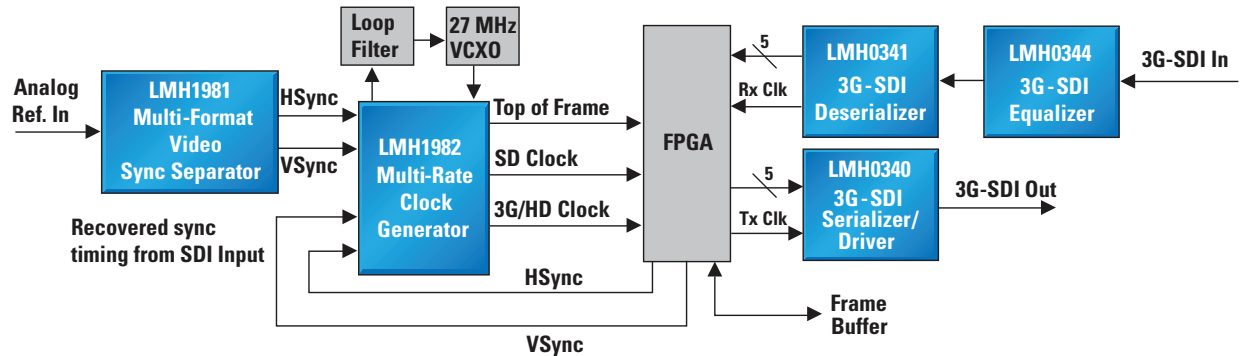
In free-run mode, the frequency accuracy of the output clocks will be based on the accuracy of the external 27 MHz VCXO. The free run control voltage of the VCXO is user defined by biasing the VC\_FREERUN input of the LMH1982.

The LMH1982 can replace discrete and FPGA PLLs with multiple VCXOs while offering low total power dissipation. With 148.5MHz output clock jitter as low as 40ps pk-pk typical the LMH1982 helps designers meet stringent system jitter specifications even when using FPGA SerDes. The LMH1982 is available in a space saving 5mm x 5mm 32 lead LLP package.

## Applications

- Video genlock
- FPGA triple rate (SD, HD, 3G) SDI SerDes
- Video capture, conversion, editing, and distribution
- Video displays and projectors
- Broadcast and professional video equipment

# Industry's Low-Jitter Integrated Multi-Rate 3G/HD/SD Clock Generator with Genlock



## LMH1982 Features

- 148.5 MHz output clock jitter as low as 40 p<sub>sp-p</sub> (typ)
- Two simultaneous LVDS output clocks with selectable frequencies and Hi-Z capability
  - SD clock: 27 MHz or 67.5 MHz
  - HD clock: 74.25 MHz, 74.25/1.001 MHz, 148.5 MHz or 148.5/1.001 MHz
- Low-jitter output clocks may be directly connected to an FPGA SDI serializer to meet SMPTE jitter specifications
- Two reference ports (A and B) with H and V sync inputs
- Supports NTSC/525i, PAL/625i, 525p, 625p, 720p, 1080i, 1080p video timing
- Output TOF pulse with programmable timing reduces required FPGA resources
- Supports cross-locking, allowing the outputs to be locked to a reference with a different timing format
- External loop filter allows control of PLL loop bandwidth, lock time, and input sync jitter rejection
- Free run or holdover operation on loss of reference
- User defined free run control voltage via VC\_FREERUN input
- I<sup>2</sup>C bus interface for programming device registers and reading device status
- 3.3V and 2.5V supplies
- 250 mW typical power consumption

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## Comparison of Alternative Solutions

Clock Generator Solution	Jitter Performance	Ease of Design	Design Flexibility	Programmable Output Timing	PCB Area
LMH1982 clock and timing generator	Best	Easy	Medium	Top of frame	Small
FPGA PLLS with multiple VCXOs	Average	Moderate to difficult	High	Many	Large
Integrated PLLS with XO/VCXO	Poor to average	Moderate	Low	None	Moderate
Digital PLL clock generator	Average	Moderate	Medium	Many	Small to moderate

