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# "The Effects of Silicon Defects on Vertical DMOS Transistors"

A National Semiconductor Quality White Paper

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Amongst other modes, the performance of a vertical DMOS transistor can be significantly degraded by silicon defects. These defects could either be inherently present in the bulk silicon in the form of excessive silicon interstitials that coalesce to form a leakage path or induced by medium to high dose ion implantation. These defects significantly reduce source to drain breakdown with concomitant increase in source to drain leakage currents.

A direct correlation has been established between observed silicon defects and low source to drain breakdowns with attendant leakage. These defects pose significant field failures and reliability issues. Fault isolation techniques were developed and customized to allow delineation of the failing vertical DMOS transistor. The authors have presented an approach toward isolating the silicon defect.

## ABSTRACT

The device under investigation is a mixed signal device consisting of mainly CMOS, Bipolar Logic and DMOS drivers. Each vertical DMOS driver is designed to supply up to 2 Amps at 40 volts for 2 msecs or 2 Amps at 22 volts for 10 msecs. These transistors are used in high voltage applications. The source to drain breakdown voltage is in the order of 80 volts. Key features of this device include a single P- well process, 5-µm n-epitaxial substrate with N+ and P+ buried layers.

Under "on" bias condition the gate is set to Vdd level with the substrate tied to ground. Electrons flow from the source contact through the N+ channel gate, through the P- body to the drain (accessible through the buried layer). E.T. measurements of a specific lot with low yield indicated that the root cause of low yield was the failing vertical DMOS transistor. Under certain bias conditions, the source was found to be shorted to drain.

## EXPERIMENT AND ANALYSIS:

EXPERIMENT 1: A product die under investigation for leakage was bench tested. The DMOS array in question was isolated using a He-Cd laser. One out of 14 sectors of the DMOS array was isolated from rest of the array. Since these DMOS transistors are connected in parallel, a defective transistor would cause the entire array to fail. The authors identified a specific DMOS transistor to be leaky. The leaky transistor was drawing in approximately 5 mA of current.

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A portion of the wafer containing this die was de-processed up to first metal layer, leaving the barrier layers intact. The barrier layer consisted of 400 Angstroms of Ti and 400 Angstroms of Ti/W( part of which was converted to TiN). After de-processing to metal-1 layer, the part was bench tested to ensure that the specific DMOS structure was still leaky.

A cluster of 8 DMOS source contacts in the identified sector was analyzed using TEM.

RESULTS: The area of concern was the annular region between the edge of gate poly and the N+ region. The failing DMOS transistor had a dislocation that crossed the P-body/N+ junction. The adjacent passing DMOS transistor did not have dislocations.

**DISCUSSION:**
The sample preparation for TEM consisted of a cluster of 8 vertical DMOS transistors. The dark center reflects presence of composite barrier layers. The defective transistor was surrounded by good vertical DMOS transistors. A plan TEM sample was prepared. Amongst several dislocations observed, the fatal dislocation was the one that crossed the P-body/N+ boundary (Figure 1). Dislocations generally are either caused by stress at the P-body/N+ junction or caused by excessive atoms originating from N+ implantation. The authors are inclined to think that dislocation caused by excessive Arsenic implantation is the leading root cause. An optimized annealing of N+ dopants is being suggested by the authors as a viable solution. Annealing would drive excessive silicon atoms (driven away by excessive Arsenic atoms during implantation) towards the surface.

**EXPERIMENT 2:**
Two parts of the product in question failed operating life test after 168 hrs. Using proprietary liquid crystal technique, thermal emission sites at the edges of the DMOS sector were identified for each part.

These parts were cleaned in a solvent contained in a beaker placed in an ultrasonic bath.
The failed sector containing the DMOS transistor in each part was isolated from rest of the circuit. This proprietary technique ensured electrical integrity of the source metal contact of the DMOS sector in question. The remaining DMOS sectors were checked for leakage. No leakage was observed confirming the failed site to be isolated. Electrical probing of the two parts indicated that the total leakage current in each part did not diminish in value after isolation.

One of the two parts was subjected to further F.A. analysis. The aluminum layer (composite M-1 layer) was selectively removed leaving the barrier layer (Ti/W) intact. SEM analysis of the contact indicated that approximately 50% of the contact area was damaged. The barrier layer along with the dielectric was chemically removed.

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**ANALYSIS OF THE DAMAGED CONTACT:**

Step by step focused ion beam milling of the contact to a depth of the drain revealed presence of tungsten. EDS analysis confirmed presence of tungsten as the residual metal. The current leakage path was through damaged silicon and remnants of tungsten ploughed through the damaged silicon into the buried layer.( Figure 2)

**DISCUSSION:**

It has been proposed that during the operating life cycle, the vertical DMOS transistor switches "on" and "off" during its duty cycle. The source voltage is set at 10 volts with the source grounded. Under these conditions, presence of silicon defect in the source contact causes further degradation leading to catastrophic breakdown of the vertical DMOS transistor. Catastrophic breakdowns could occur in any DMOS cell that has silicon defect. For the device in question, maximum electric field occurs at the edges of the DMOS sectors. The operating life failures have been observed at the edges of the DMOS sectors.

**CONCLUSION**:

The silicon defects identified through two separate methods caused significant leakage currents and device failure. The device partitioning technique described in this paper has proved successful in pinpointing and identifying the nature of the failure.

Lattice dislocation existing across pn junctions of vertical DMOS transistor cause leakage. Under stress conditions these lattice dislocation can degrade and further damage the device.

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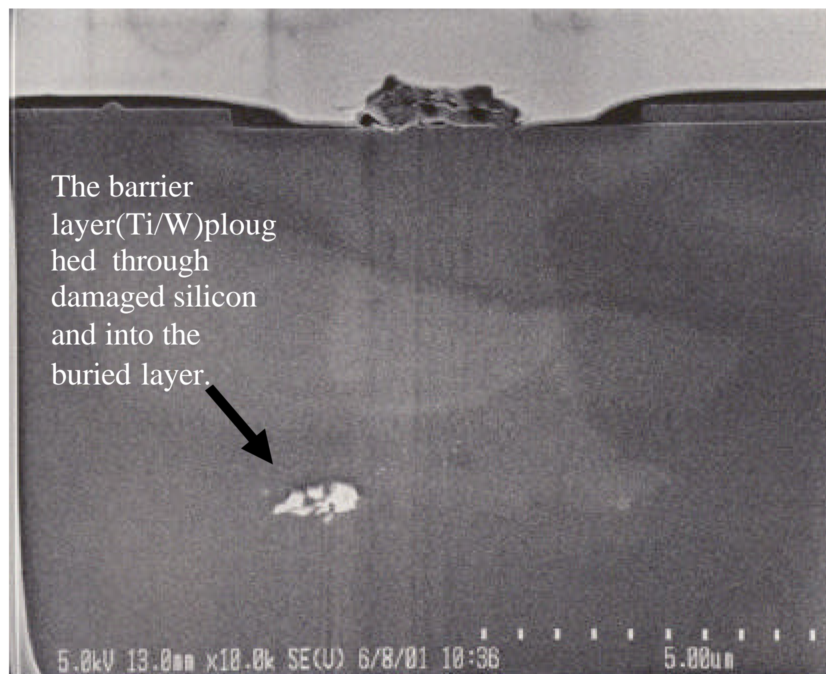


Focused ion beam cross section across the damage silicon at the top.
Note: presence of Ti/W barrier layer approximately 5um from top of the silicon surface

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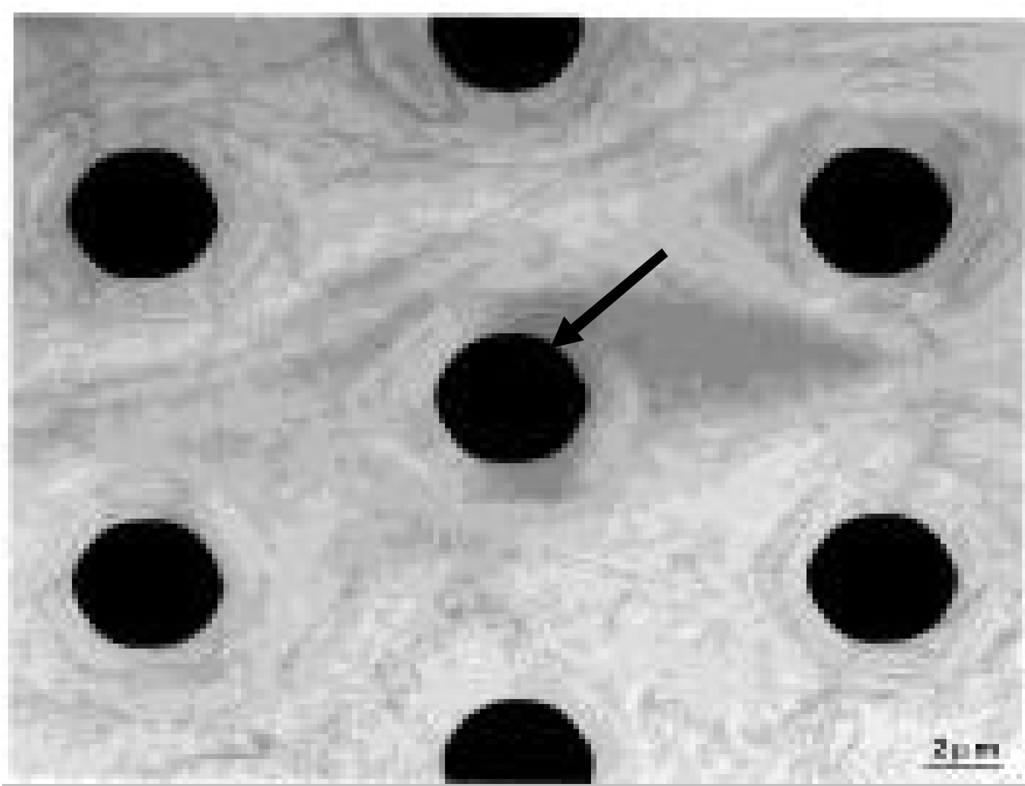

TEM analysis of cluster of DMOS array consisting of a failed transistor surrounded by good transistors (see arrow)

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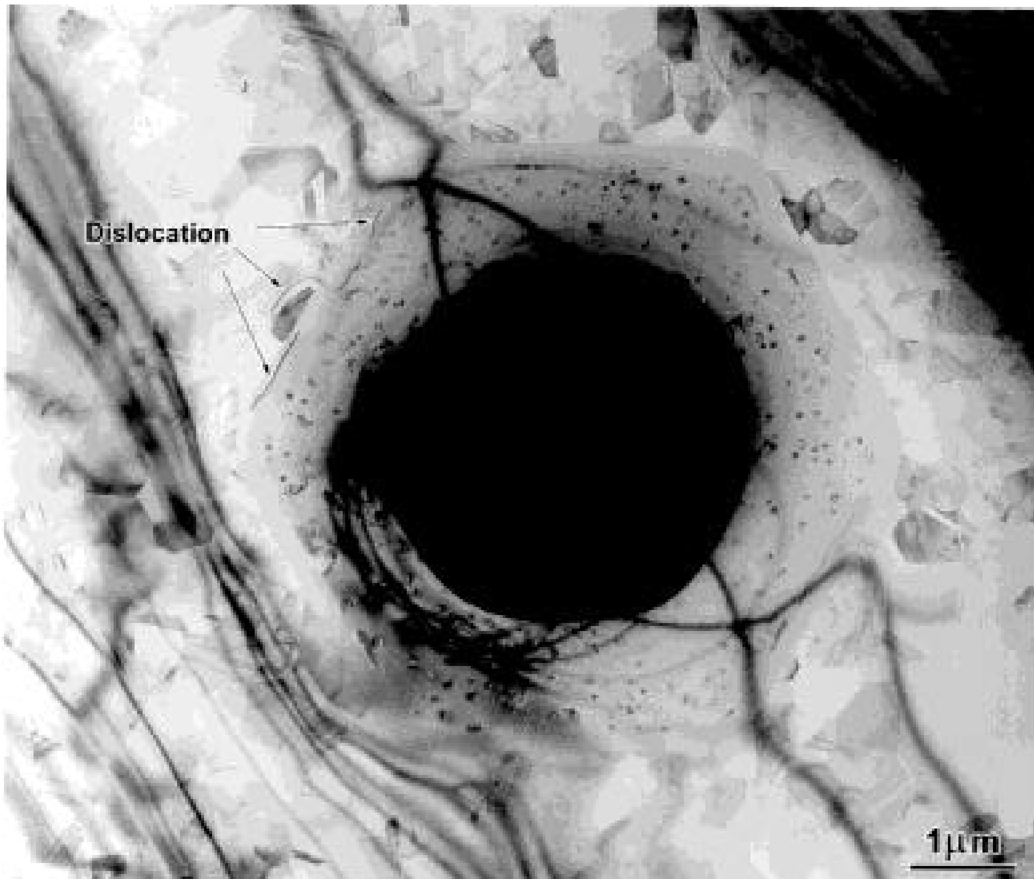


FAILED TRANSISTOR WITH DELINEATED DISLOCATION LINE CROSSING P-BODY/N+ JUNCTION