

## **“Antenna Ratio (‘Antenna Rule’) Violation Causing ‘Super I/O’ Device Failure Affecting Both Yield and Reliability Stress Results”**

A National Semiconductor Quality White Paper

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### **Abstract**

Design Rule Check (‘DRC’) provides assurance that the design and layout of a device are compatible and will not lead to device failure during normal operation or production of the device. The analysis process which led to the modification of the corporate CMOS7 antenna DRC rules and device layout for the ‘Super I/O’ device will be discussed. Failures were generated during Early Failure Rate (‘EFR’) reliability stress which were found to be related to Yield failures. Failure analysis results indicated these failures were all on specific transistors in one circuit cell. This revelation led to the modification of the corporate DRC run set on antenna rule. Slight changes to the product layout were also made to follow the modified rule. The reliability and yield failures were eliminated.

### **The ‘Antenna Effect’**

#### **Failure Mechanism**

Modern fabrication flows use plasma etching as an integral part of some process steps. The plasma etching systems create and sustain an energized and highly ionized state of matter in order to etch or deposit layers onto silicon wafers. As a result of this exposure, charges can build up on circuit areas. Ion implant equipment can also cause charge build up. Uncontrolled discharge of these charges may cause

permanent physical damage to the physical structures on the device, e.g., transistor gate oxide.

#### **‘Antenna’ and ‘Antenna Ratio’**

The propensity for damage to the circuitry on a wafer can be exacerbated by the existence of ‘antenna’ structures. The ‘antenna’ is an interconnect, i.e., a conductor like polysilicon or metal, that is not electrically connected to silicon, i.e., not ‘grounded’, during the processing steps of the wafer. The connection to silicon would normally provide an electrical path to bleed-off any accumulated charges. If the connection to silicon does not exist, charges and may build up on the interconnect to the point at which rapid discharge does take place and permanent physical damage results, e.g., to MOSFET gate oxides. This destructive phenomenon is known as the ‘antenna effect’.

The ‘antenna ratio’ of an interconnect is used to predict if the antenna effect will occur. ‘Antenna ratio’ is defined as the ratio between the physical area of the conductors making up the antenna to the total gate oxide area to which the antenna is electrically connected. A higher ratio implies a greater propensity to fail due to the antenna effect. This can result either from a relatively larger area to collect charge or a reduced gate oxide area on which the charge is concentrated.

#### **Safeguards**

A number of techniques can be utilized to minimize the antenna effect. For example, the occurrences of antennas can be predicted and their ratios calculated using design verification and layout software known as ‘design rule check’ (‘DRC’) programs. Then by adjusting the physical layout of the interconnects, the antenna ratios can be reduced to an acceptable level. A ratio of 100:1 is a typical design rule upper limit. In addition, processing steps utilizing plasma can be optimized to reduce the build-up of charges on any antennas that do exist on devices.

### Device history

Concerns were raised regarding the existence of a reliability problem and the production worthiness of the PC97307 “Super I/O” device following the failure of samples during “Early Failure Rate” (EFR) production burn-in. The devices had been built with NSME 5-volt CMOS7 process and assembled in NSSG. CMOS7 utilizes a 0.5- $\mu$ m minimum feature size, three metal layers, a single polysilicon layer, and an epitaxial (‘epi’) layer in the silicon.

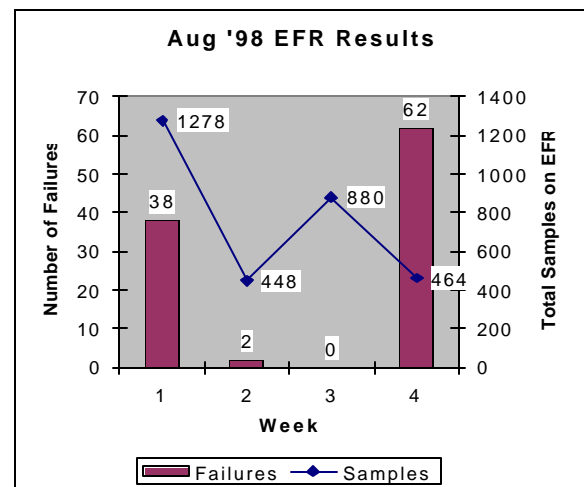
The PC97307 had been granted full production release based on acceptable reliability test results. Process changes had occurred during the initial stages of the NSME CMOS7 process qualification. However, 10 sequential die runs had subsequently generated 1 failure out of a total sample size of 1800 devices.

An EFR monitor, i.e., 48-hour Dynamic Operational Life (DOPL), was then begun to monitor production of the device. The first few lots generated failures. Additional failures were generated as additional lots were sampled (1 wafer per lot; lot released only when EFR result was zero failures).

#### Initial Early Failure Rate (‘EFR’) Results

Results from the initial month of EFR screening (July ’98) presented a puzzling view of the reliability performance of the device. The occurrence of failures was not expected, nor was the variability of the magnitude of the problem. The first groups of parts had been run as ‘EON’ (Engineering Order Notification), prior to the release of the device to production to insure proper engineering controls. Table 1 displays the performance data of the EFR lots.

Die Run Number	Sample Size	Failures	Burn-In Date
1	144	0	01Jul
2	150	10	09Jul
2 (repeat)	150	1	14Jul
3	144	7	25Jul



4	144	1	28Jul
5	144	0	28Jul

Table 1: Early EFR Performance

During August of 1998, the variability of the results continued as more lots were monitored via the EFR sampling. During any given week, the number of failing lots never numbered more than two, i.e., failures were generated from distinct lots and not across all lots.

Figure 1: Variable EFR Performance in August 1998

A cross-site and multi-functional team was formed to resolve the issues. Team members represented National Semiconductor sites in Israel (NSTA), Singapore (NSSG), Maine (NSME), and Santa Clara (NSSC).

## Investigating the problem

### Identifying the Failure Signature

All of the parts placed on EFR stress had been fabricated at NSME on the CMOS7-5v process, assembled in NSSG, then stressed and tested at NSSG. Failures had occurred in both the 'Production' and 'Reliability Lab' burn-in systems at NSSG. Only a limit number of lots had failed units, but when failures did occur, there tended to be many, e.g., more than 3. This pattern implied that the failure mechanism was lot dependent.

The common failure mode as measured by production ATE (Automatic Test Equipment) was a failure during the 'FDC104' test sequence on D7 (pin 99). 'FDC104' is functional test of one of the major components of the device, i.e., the floppy disk controller, and occurs towards the middle of the test program for the PC97307. Occasionally 'Iccsb' (stand-by supply current) failed at readings from 400 $\mu$ A to 5mA.

### Device-level or Failure analysis ('FA') results

Initial FA results indicated a correlation between the FDC failures and the appearance of fused metal (aluminum) near the circuitry close to the D7 bond pad; a Schmitt Trigger cell ('GPTTLSMTX6\_TA50'). In addition, damage to the gate polysilicon and oxide, and contacts were noted. These findings were duplicated at the several sites performing die level analysis. Analysis details follow.

### Curve trace

In addition to the ATE failure mode, curve trace techniques were also able to detect a difference between failing and passing units. Leakage or shorted characteristics between Vcc and Ground ('GND') were measured on many devices (see Figures 3 and 4 for representative examples).

### Die Surface Inspection

For many cases, physical damage, i.e., fused aluminum, was visible in circuitry near the failing pin. In other cases, liquid crystal techniques were required to aid the fault isolation (see Figure 4). Emission microscopy analysis was also successful in some instances, but consistent results were not obtained, i.e., some failures did not have an emission

site. Figure 5 displays the appearance of the circuit area with all layers intact.

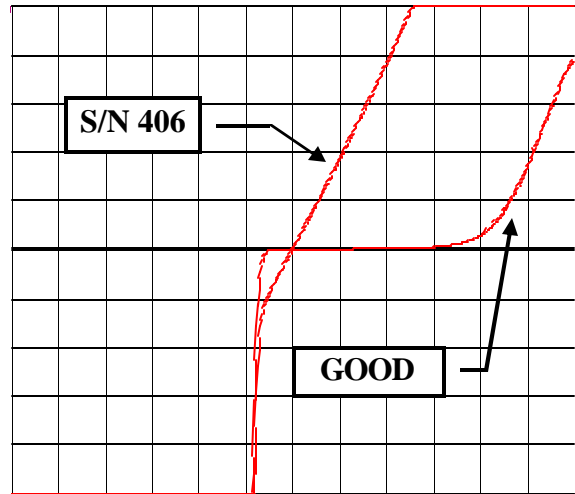


Figure 2: Device failed FDC104 and Iccsb = 2.5-mA

Horizontal = 0.5-volts / division

Vertical = 100- $\mu$ A / division

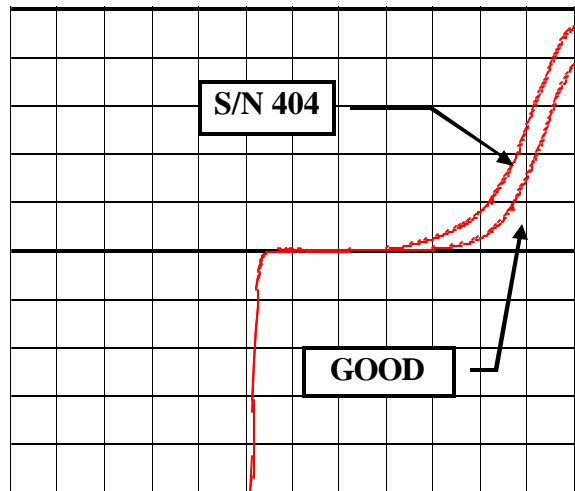


Figure 3: Device failed FDC104 and

Iccsb = 600 $\mu$ -mA

Horizontal = 0.5-volts / division

Vertical = 100- $\mu$ A / division

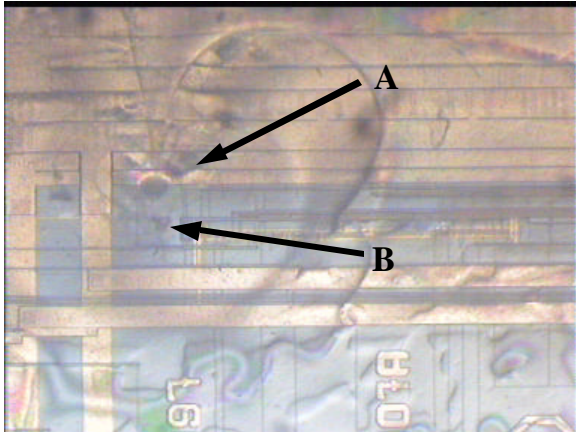


Figure 4: Liquid crystal analysis 'hot spot' at Site A

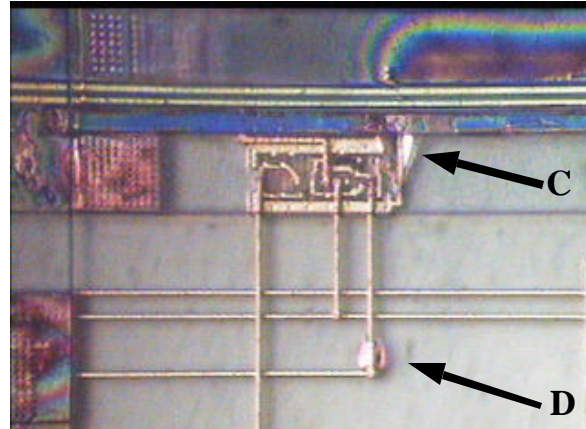


Figure 6: Optical view after top metal was removed  
Note: Fused aluminum exists at two sites and Site D is the same location as Site B in Figure 5

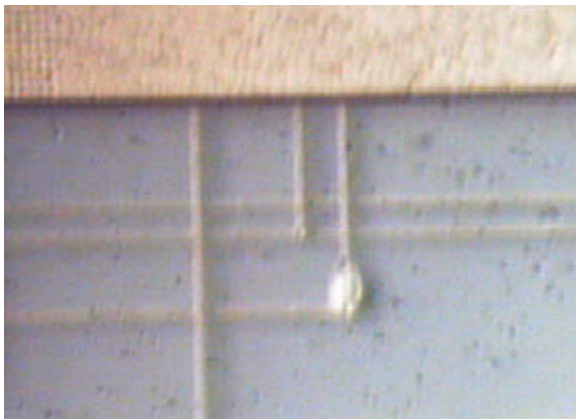


Figure 5: Detail of fused aluminum at Site B in Figure 4

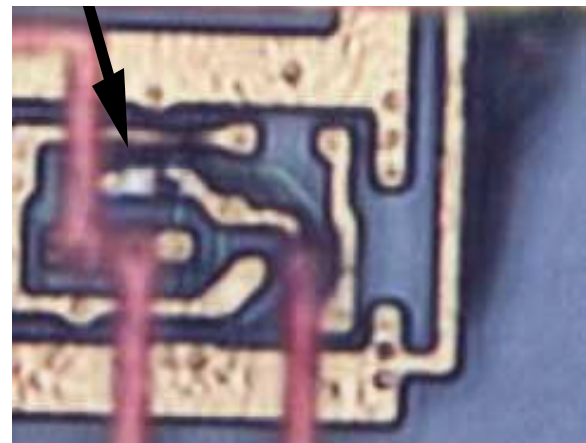


Figure 7: Example of alternate site of fused aluminum near Site C  
Note: View is of a different device than in Figure 6

#### Post-deprocessing Inspection

Passivation and the top metal layers were removed to facilitate the inspection in the Schmitt Trigger circuit area for any damage to the portion of the circuitry underneath the wide metal busses. Damage in the form of fused aluminum was observed on failing devices. Figures 6, 7, and 8 are views on different devices, but in the same area. A 'parallel polish' technique was used to remove the top layer of metal.

The specific location of the metal damage varied. In addition, deprocessing on sample failures revealed gate oxide ruptures in a particular PMOS transistor identified as 'P4' in the Schmitt Trigger cell, which is connected to the PWD port.

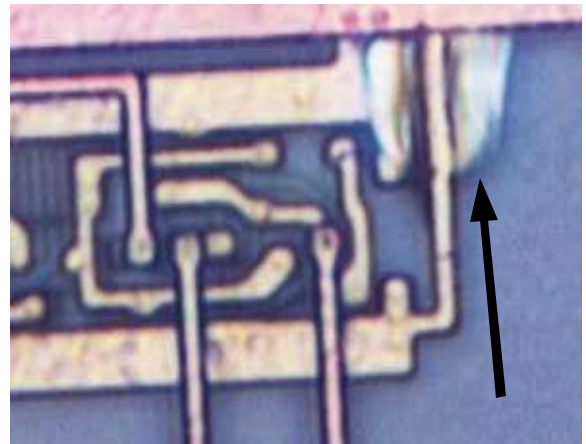


Figure 8: Another example of fused aluminum damage at Site C

0.5µm wide and approximately 6µm long; which produced the enormous area differential of 9200.

**Circuit Considerations**

Figure 9 shows a cell-level diagram of the Schmitt Trigger circuit. Only the cell external ports are shown (PWD and PWDHL), along with two of the cell transistors. The PWD and PWDHL controls are used to enable the Schmitt Trigger operation and to set the output when disabled. In the particular application of the Schmitt Trigger cell for this pin, the PWD port was grounded (connected to Vss). Also, the PWDHL port was connected to the positive power supply (Vdd). There were a total of 44 Schmitt Trigger cells in the device that had their PWD signals connected to ground.

‘Wafer-to-wafer’ and ‘edge versus center’

Not only was the damage site repeatable, the electrical failure signature, ‘FDC104’, was also repeatable. There was a low-level wafer yield ‘hit’ (< 1%) as a result of this test. The uniqueness of this electrical signature was utilized to track the performance on a wafer-to-wafer basis. Experiments that tracked the source wafer numbers found the failure to be wafer-to-wafer, not just lot-related.

Additional experiments investigated the correlation of a failed die with respect to its placement on the wafer, e.g., edge versus center on the wafer.

An ‘edge die’ was defined as a die being no more than 2 dice away from the edge of the wafer. A ‘center die’ was contained in 14x14 matrix of dice located in the center of the wafer. Several wafer lots were sampled and stressed over the course of 2 weeks. A strong tendency for FDC104 failures to occur on dice picked from the edge of the wafer was indicated (see Table 2)

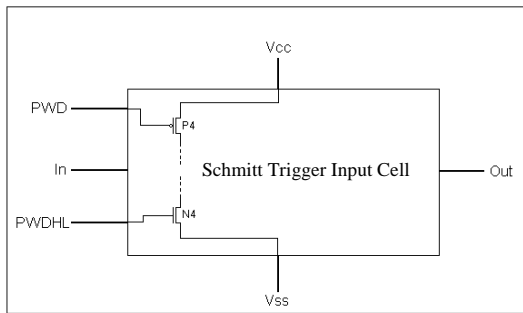


Figure 9: Schematic Diagram of the Schmitt Trigger Input Cell

**Areas of Investigation**

**Antenna Effect**

The repeatability of the damage site led to the belief that the failure was layout-related. Specifically, an antenna effect was suspected to have led to the damage of the gate of P4 and the fused metal interconnects. P4 was connected to the PWD port, which in turn was connected to a Vss metal bus. A careful evaluation of this connection led to the realization that this portion of the Vss bus was not connected directly to silicon until the top-layer metal was deposited.

The antenna ratio of this PWD connection was checked and found to be 9200:1. PWD was connected to Vss using second-layer metal (“M2”) which was 1700µm long and 35 µm wide. The gate oxide was

Lot ID	Wafer ID	Placem nt on Wafer	# of Failures	# of Samples
1	A	Edge	19	189
1	A	Center	1	189
1	B	Edge	13	189
1	B	Center	0	193
2	C	Edge	0	193
2	C	Center	0	176
2	D	Edge	0	193
2	D	Center	0	197
3	E	Edge	7	193
3	E	Center	0	185
4	F	Edge	6	193
4	F	Center	1	196
	<b>Total</b>	<b>Edge</b>	<b>45</b>	<b>1150</b>
	<b>Total</b>	<b>Center</b>	<b>2</b>	<b>1136</b>

Table 2: ‘Center versus Edge’ Wafer Study

The FDC104 wafer sort failures also failed at the same pin (D7) and had the same failure signature of parts that failed during EFR. Good lots had a lower incidence of FDC failures.

#### Other Areas of Investigations and Findings

A number of additional investigations and experiments were performed to investigate other failure mechanisms:

**Fabrication-related** - The fab histories of the failing lots were compared with passing lots. No differences or trends were detected in oxide integrity and yield data, except for the FDC104 signature.

Splits were run on suspect processing systems, e.g., metal etch and TEOS deposition. Systems were also placed in 'high-plasma' conditions, i.e., configurations historically known to cause the greatest amount of plasma damage, as part of this study. No clear evidence could be found to indicate that any particular system was primarily responsible for causing the failures.

Analysis by Scanning Ion Microprobe Spectroscopy ('SIMS') confirmed the starting material to be 'epi' versus 'non-epi'. The lack of 'epi' would degrade the robustness of the device to electrical 'latch-up'.

A reticle analysis, i.e., visual inspection, on the mask set did not reveal any defects or unusual artifacts.

A cross-section in the area of failure on failing and passing units did not reveal any cause for device failure.

**Burn-in and handling-related** - Unstressed devices from failing lots were subjected to simulated electrical overstress ('EOS') and electrostatic ('ESD') voltage transients. The failure signatures for these units were different, e.g., high Iccsb and failed almost all test patterns unlike the EFR failures which failed only the FDC104 pattern. Physical damage was also observed to be different than on the EFR rejects.

Any sensitivity to the 'test pattern' used during EFR stress was examined. The failing external pin was always connected ("hard-wired") to Vdd through a high resistance, i.e., a discrete resistor, on the burn-in board and not exercised uniquely or more than any other similar pin. These other pins that did not fail were connected to Vdd in the same manner.

The existence of voltage transients in the burn-in system was checked. No transient events were detected.

The burn-in board schematic and handling procedures were checked. This included verifying the specified stress condition, revision history, and component values, e.g., capacitors and noise suppression devices.

### Fixing the Problem

Initially, the team decided to take two significant actions towards implementing corrective action:

- 1) 'Ink out' edge die on suspect wafers, and
- 2) Create a mask change that would significantly reduce the antenna ratio for the D7 circuitry.

#### Containment - 'Inking Out' Strategy

Because the occurrence of failures was wafer-dependent, there was an initial concern that the sampling methodology used for EFR may not have sufficient visibility of all wafers within a given lot to insure the desired reliability levels of the lot. The following 'ink out' procedure was instituted at wafer sort; 'ink out' being the marking of a die as unusable. If a wafer had more than 1 die with an FDC104 failure, then all edge dice would be 'inked out'. If performed, this 'inking out' of edge dice would reduce the total number of available die on a wafer by 22%. An example of the overall impact of this procedure was that for the first few lots, 37% of all wafers were inked out. This meant that a total of 8% of all dice were inked out.

#### Address Root Cause - Mask Fix

After considering a number of options, the mask was fixed by making 3 modifications on only two layers of the mask set existing at that time:

- Modification 1: Enlarge the M1 width at the site of new via1
- Modification 2: Add new via 1 connecting PWD node to Vss in M2
- Modification 3: Delete M1 interconnect leading to Vss antenna

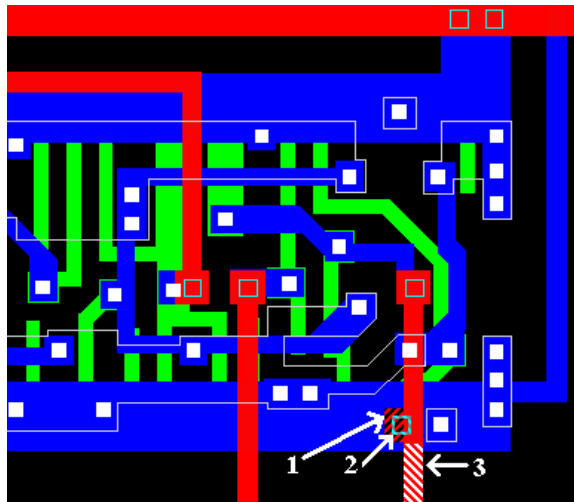


Figure 10: Layout representation of the modifications to M1 and Vial mask

#### Post 'Mask Fix' Results

The effectiveness of the mask fix was monitored as the new mask set produced wafers. Not all of the FDC104 rejects were eliminated, but the percent of wafers rejected dropped from 38% to 22%, i.e., reduced by almost half.

The EFR failures that had been eliminated by the mask fix had been caused by an antenna effect on transistor P4 of the Schmitt Trigger. The gate oxide of P4 would have been weakened prior to EFR stress. Then, during the dynamic operational life (DOPL) burn-in, current would have flowed through this weakened gate from Vdd (connected to the source of P4) to Vss via the PWD line (the PWD input was disabled in the circuit design by being connected to Vss). Increased current levels would occur as additional physical damage occurred in the gate oxide. The current levels would reach a point at which the metal interconnects would melt and caused the physical damage noted during initial FA.

Analysis of the rejects not addressed by the mask fix determined that fused metal and gate oxide ruptures had occurred in the same Schmitt Trigger cell, but on different pins or on different transistors. The gate oxide ruptures were located in the gate of transistor 'N4'. Transistor N4 was connected to PWDHL, which in this application was connected to Vdd. The antenna ratio of PWDHL was found to be 3200:1.

#### Pursuing the Antenna 'lead' (Follow-up Work)

The antennas and their ratios were studied carefully on the PC97307. Another mask change was

performed to address failure sites that had been determined to be antenna-related. A single-layer change to M2 was all that was required to accomplish this.

Due to the relationship with the external customer and the anticipated lifetime of this product, an all-inclusive fix involving many more layer changes was not performed. This would have involved adding metal and poly 'jumpers' which would have required changing the via masks as well as for the conductors, and possibly adding diodes, involving even more mask changes. All antenna ratios would then be reduced to below 100:1 for antennas not connected to diodes, this target ratio being defined by design guidelines. There were approximately 90 such antennas identified on the device, with the largest having a ratio of 1050:1.

The wafer sort and EFR results on the devices were monitored following the implementation of the 'new' mask fix. Lot yields were greater than 90% and no failures occurred in EFR stress. As a result, the 'edge inking' was discontinued, which helped realize a cost saving of approximately \$600k per quarter. Eventually, 10-straight lots passed EFR without a single failure of any type.

## Learnings

### Mask changes

The team had decided to implement a mask change to reduce the antenna ratios of the Schmitt Trigger cell of pin 99. A 'quick fix' in the way of correcting the database that was used to generate a new mask, i.e., modifying the 'fractured database', was done. A parallel and more time consuming effort to follow standard 'tape out' procedures ending in mask generation was also started. This slower process would be more in compliant to existing design process protocols. When finished, the revised masks from the tape out process replaced the 'quick fix' masks in production. The 'quick fix' masks were then physically destroyed.

### Antenna Ratio DRC

A 'loophole' existed in the set of DRC rules used at the time of chip design. If a node was connected to power supply lines, i.e., Vss or Vdd, then the antenna for that node was ignored, whether the supply was physically connected to silicon or not at the time that the layer was being processed.

An enhanced set of DRC rules detecting antenna violations was developed. Extremely large antennas did originally occur in the PC97307 because PWD, an input gate, was sometimes connected to supply busses in second-layer metal ('M2') which were not connected to silicon during wafer processing. This DRC flaw that allowed the PWD (and other) antenna violations to occur, was eliminated in the enhanced set of DRC rules.

The 'enhanced DRC' identified groups of two additional significant violations: 1) A Pin 99 port connected to Vss, and 2) Ports from pins 102, 103, 104, and 105 connected to Vdd (antenna ratios greater than 3200:1). Damage due to these antennas was observed in EFR failures, but not as often as the Pin 99 locations.

An additional mask set revision fixed these large antenna violations, but only after a careful review of analysis findings. An effective and cost efficient solution to insure device reliability was implemented, involving input from the external customer.

Previously undetected violations were detected when the enhanced rule set was applied to other device types in the Super I/O family.

Mask changes were not made for these devices, but test patterns were added to detect any antenna-related failures for sensitive nodes.

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