



# How to create designs with Dynamic/Adaptive Voltage Scaling

Roy H. Liu

National Semiconductor Corporation

# What you will learn from this session

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- Design challenges with variable voltage level
- Design partitioning guidelines for voltage scaling
- Level shifting strategies
- Dealing with the variable timing
- A voltage scaling design example

# Frequency and Voltage Scaling for Power Saving

$$P = \alpha C V_{DD}^2 f_c + V_{DD} I_{off}$$

Dynamic or AC power:  $\alpha C V_{DD}^2 f_c$

Static or DC or leakage power:  $V_{DD} I_{off}$

P = power

$\alpha$  = activity factor

C = capacitance, proportional to the number of gates and routing parasitics

$V_{DD}$  = supply voltage

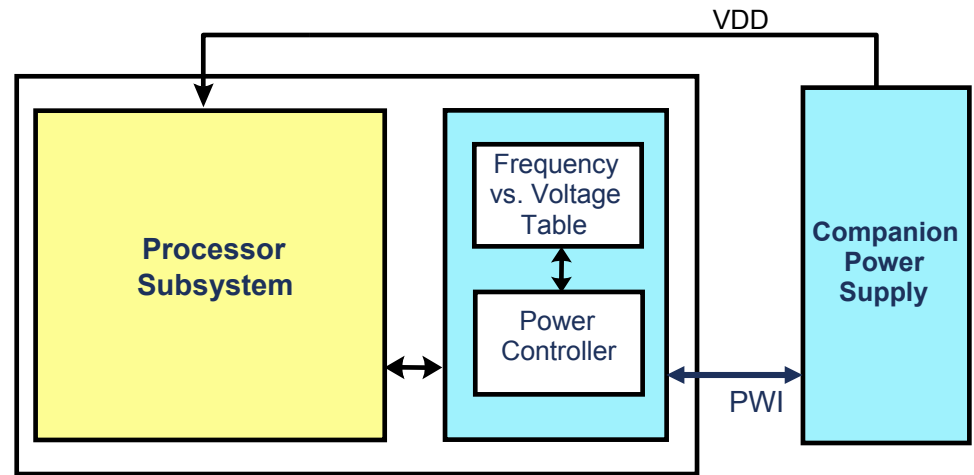
$f_c$  = operating frequency

$I_{off}$  = leakage current, proportional to the number of gates, increases with reduced threshold voltages (smaller gate lengths)

# DVS and AVS

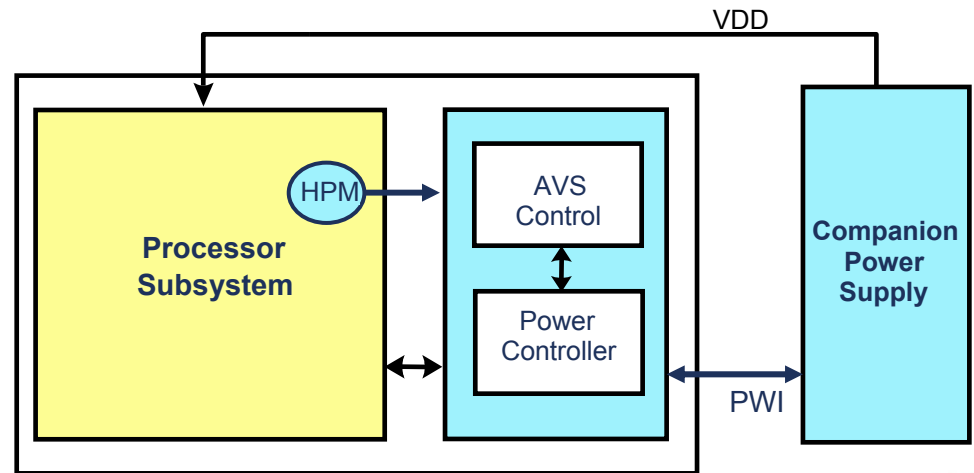
## ■ Dynamic Voltage Scaling

- Open-loop voltage scaling
- Voltage level determined by clock frequency based voltage table



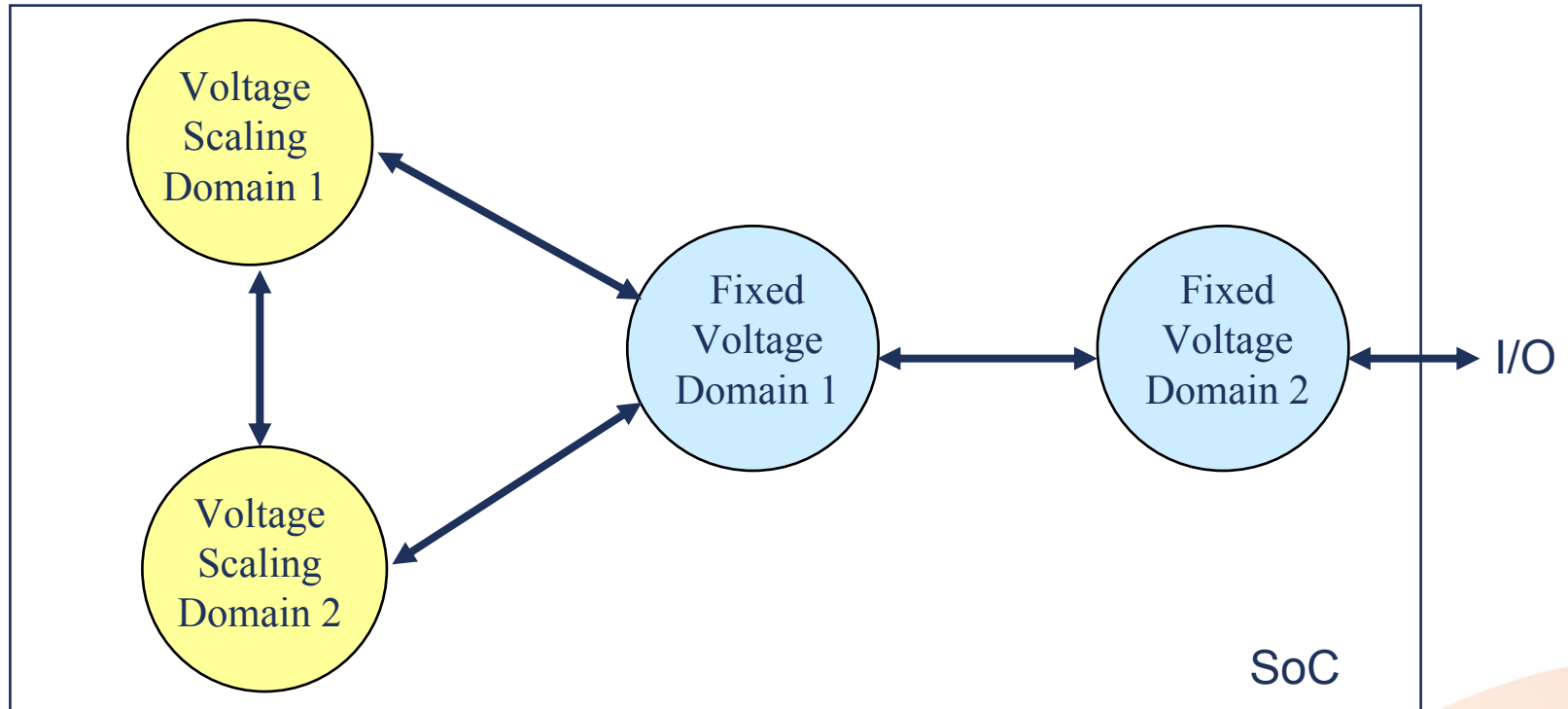
## ■ Adaptive Voltage Scaling

- Closed-loop voltage scaling
- Voltage level determined by voltage control loop



# Voltage Domain Interfaces

- Between two different levels of fixed voltage domains
- Between a fixed voltage domain and a voltage scaling domain
- Between two independent voltage scaling domains



# What is different with Voltage Scaling Designs

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- Signals going across voltage domain boundary require level translation to be recognized correctly in the destination domain
- Signal timing across voltage domain boundary varies with the voltage level
  - DVS – can be predicted with multiple voltage points analysis but may not be practical
  - AVS – not predictable

# Design Considerations for DVS/AVS Designs

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Three areas to focus on:

- Voltage domain and design partitioning
- Level shifter insertion
- Timing across voltage domain boundary

# Voltage Scaling Domain Partitioning

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- Voltage scaling goes together with clock frequency scaling
- Clock domain boundary is naturally the choice for the voltage scaling boundary
- No tricky timing problems to worry about if the boundary is an asynchronous interface
  - Synchronous interface at the voltage scaling domain boundary is required in some cases

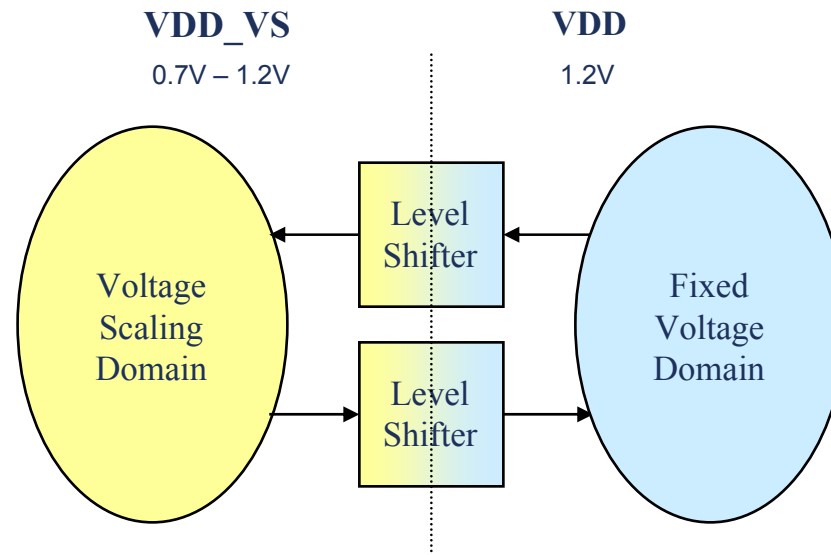
# Integrate IP Blocks for Voltage Scaling

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- IP block with single clock domain – use it as is, add appropriate level shifters outside of it
- IP block with multiple clock domains
  - Example: an internal bus interface clock that scales, an external peripheral clock that does not scale
  - Re-partition the IP to facilitate voltage domains separation and level shifter insertion
  - Over-design to ensure proper operation at minimum voltage scaling level
  - Keep it outside of voltage scaling

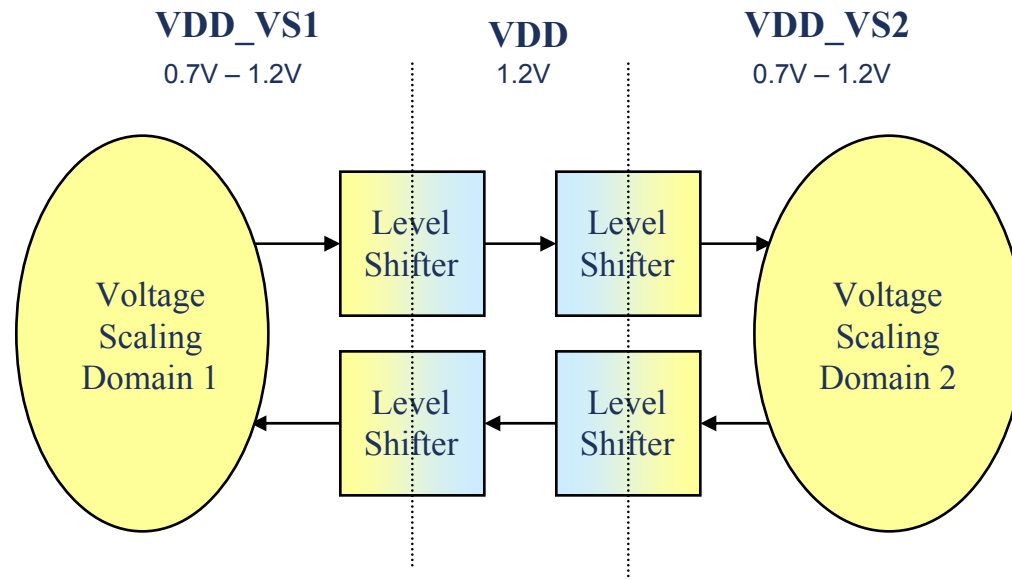
# Level Shifting between Voltage Scaling Domain and Fixed Voltage Domain

- From voltage scaling domain to fixed voltage domain – level shifting up
- From fixed voltage domain to voltage scaling domain – level shifting down



# Level Shifting between Voltage Scaling Domains

- Use variable voltage to variable voltage level shifters
- Always up-shift to fixed voltage domain and then down-shift to the other voltage scaling domain

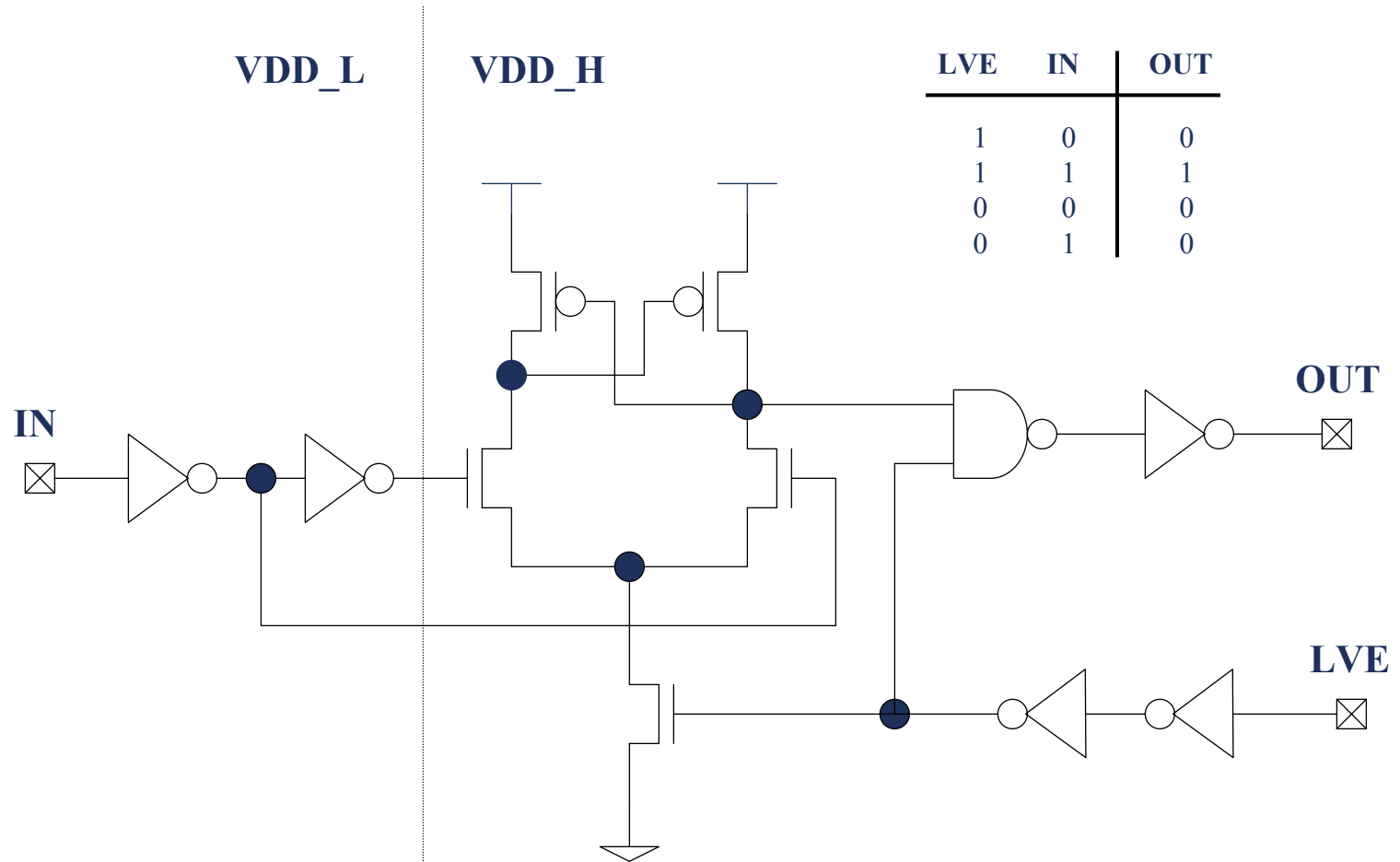


# Signal Clamping in Power-down

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- Clamp all outputs from powered down domain during power down to prevent leakage and erroneous data writing in the destination voltage domains
- Clamp all inputs to powered down domain during power-down to prevent latch-up
- Combine signal clamping function in level shifters

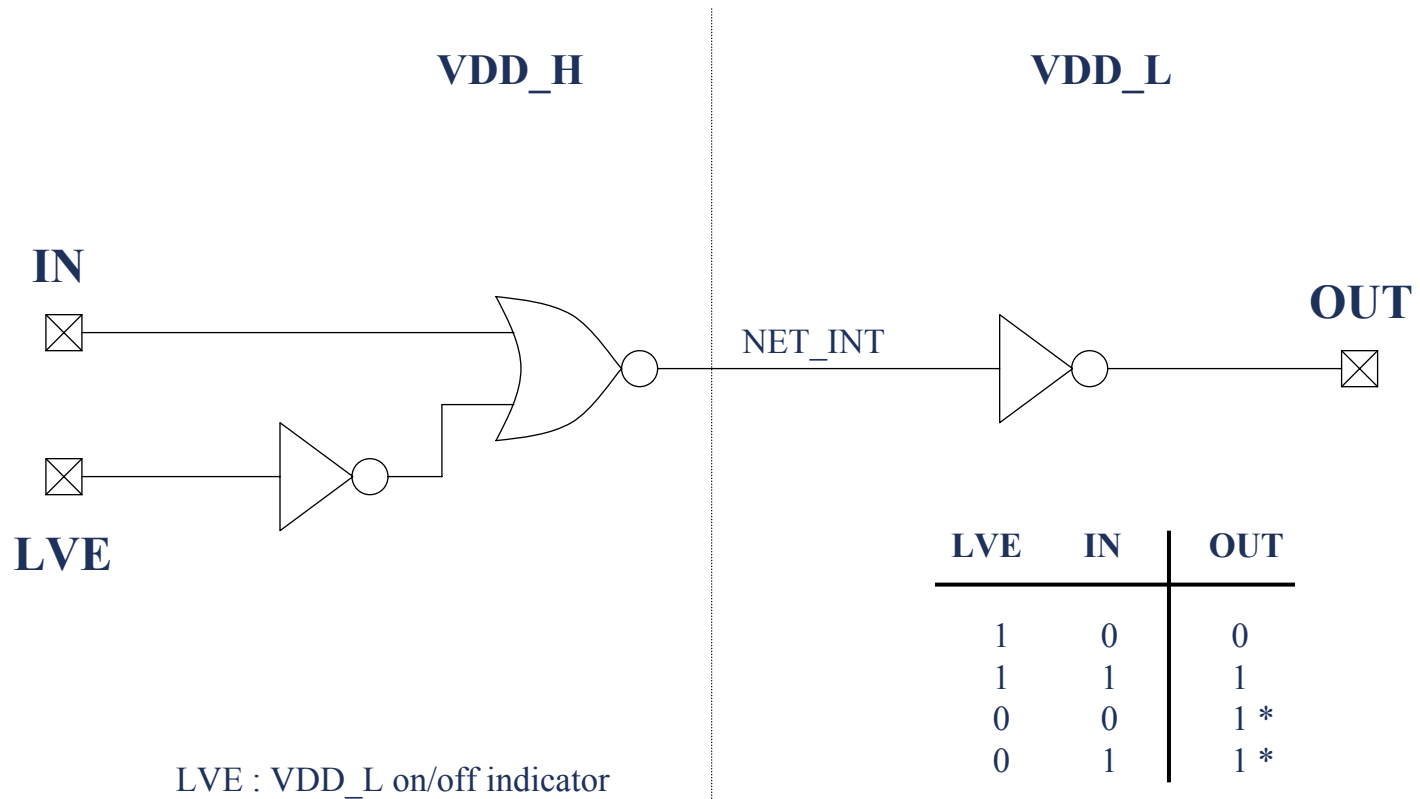
# Up-shifting Level Shifter with Clamping



LVE	IN	OUT
1	0	0
1	1	1
0	0	0
0	1	0

LVE : VDD\_L on/off indicator

# Down-shifting Level Shifter with Clamping



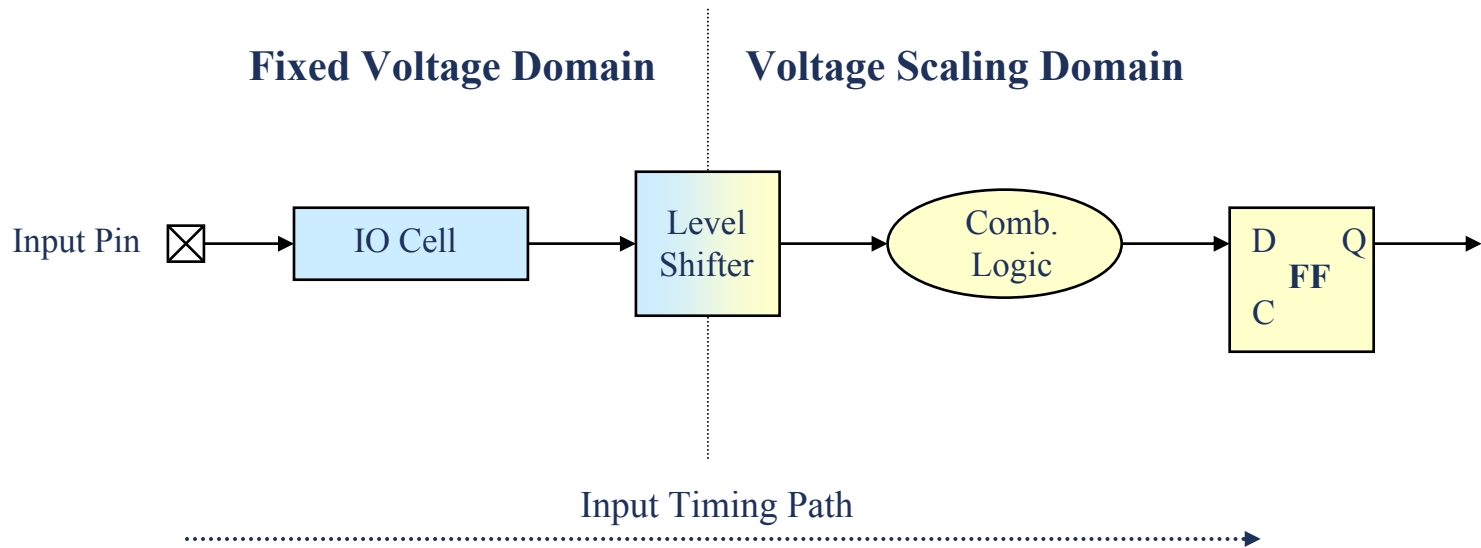
\* OUT is unknown and NET\_INT is driven low when VDD\_L is off

# Voltage Scaling Clock Switching Considerations

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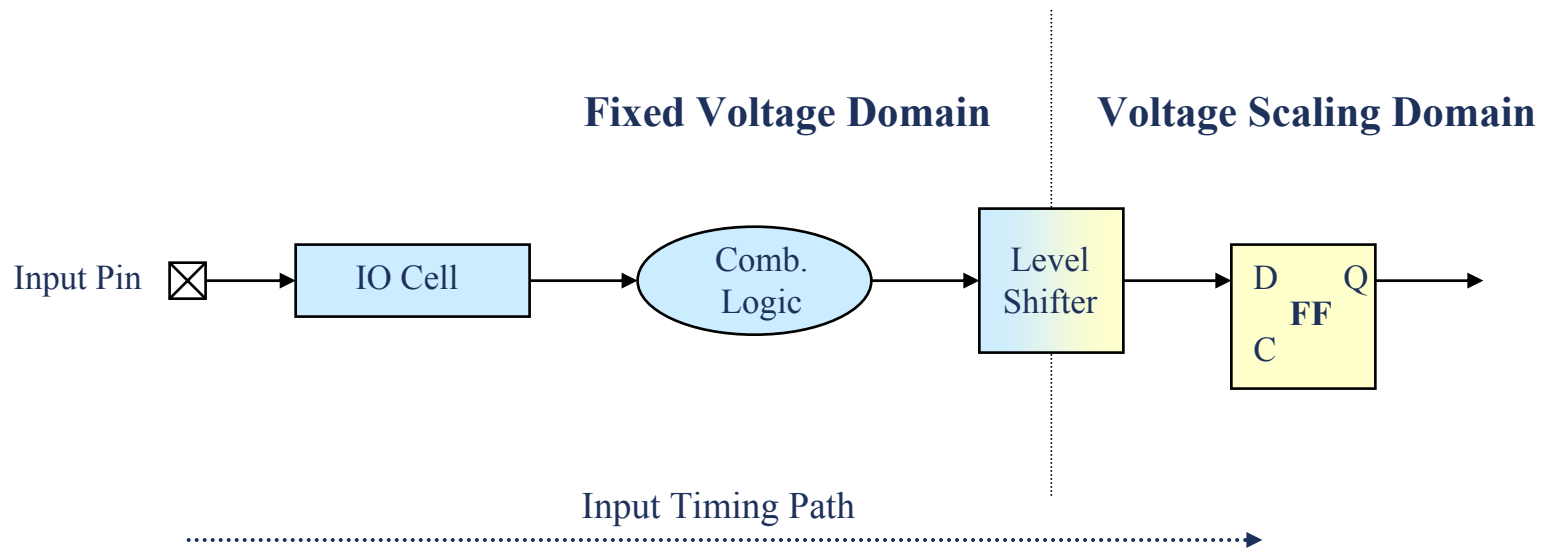
- Scaling up the clock frequency – voltage level must be sufficient before the clock can be switched to the new frequency
- Scaling down the clock frequency – clock can be switched to the new frequency right away as the voltage level is already sufficient

# Input Timing Voltage Scaling Implication – Scenario 1



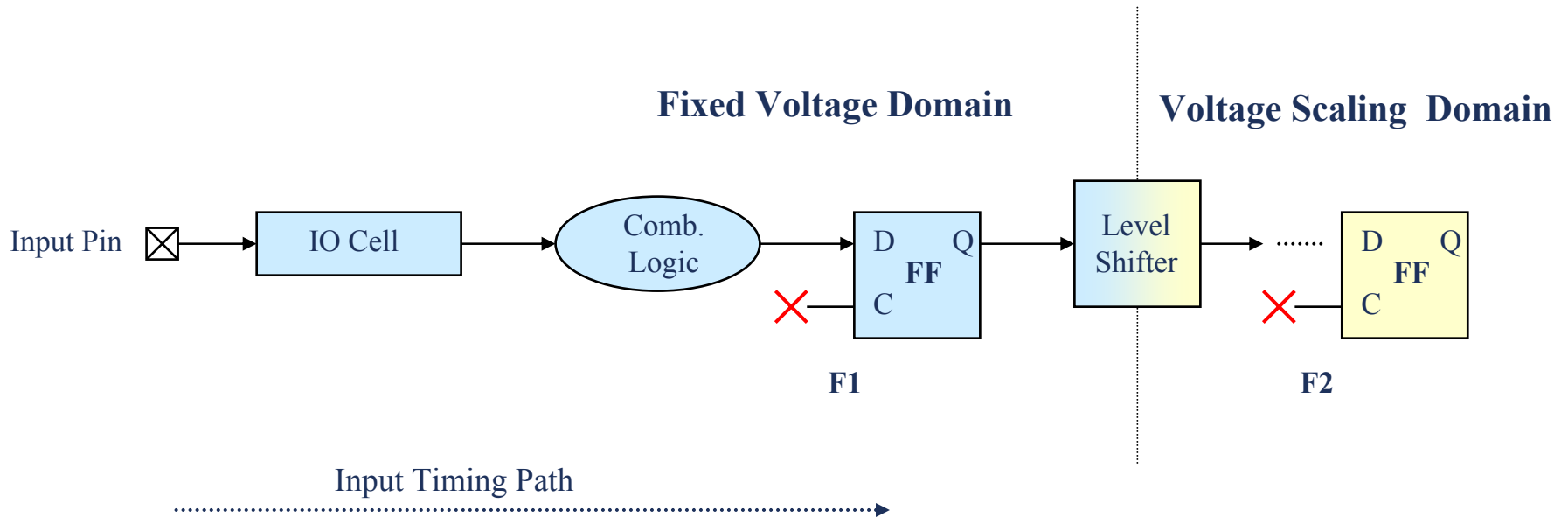
Input setup/hold timing may vary substantially over voltage scaling range depending on the amount of logic in between level shifter and latching flop.

# Input Timing Voltage Scaling Implication – Scenario 2



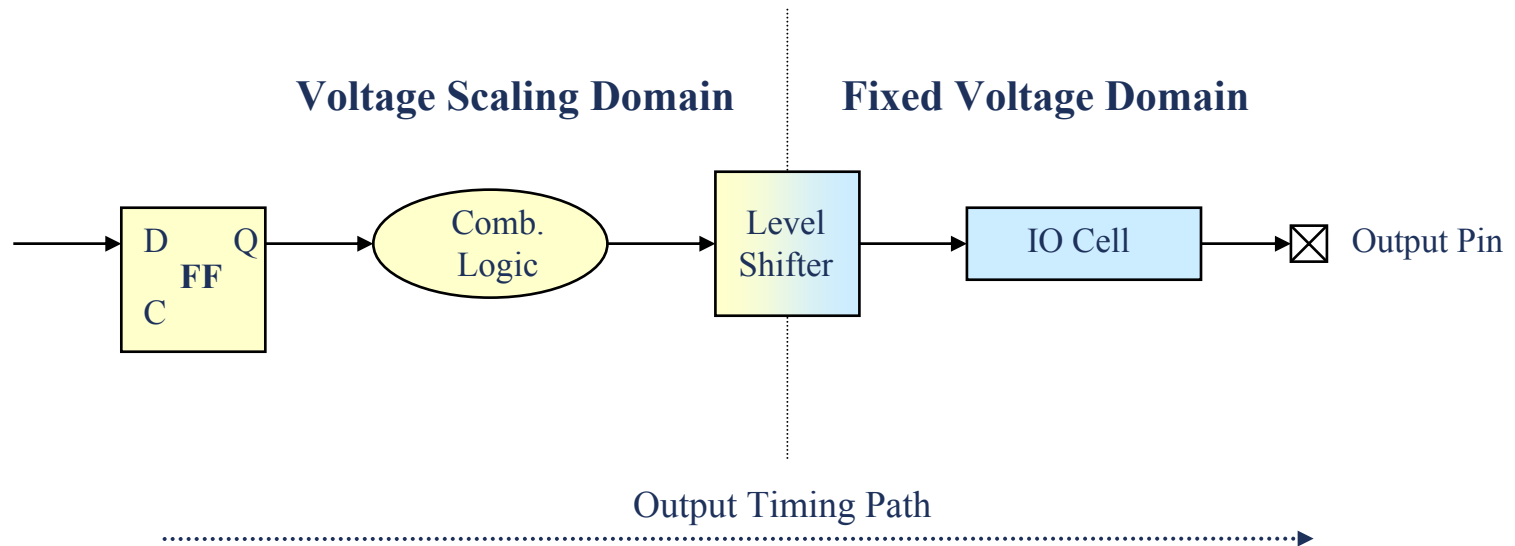
This voltage domain partition gives smaller setup/hold time variation over voltage scaling range.

# Input Timing Voltage Scaling Implication – Scenario 3



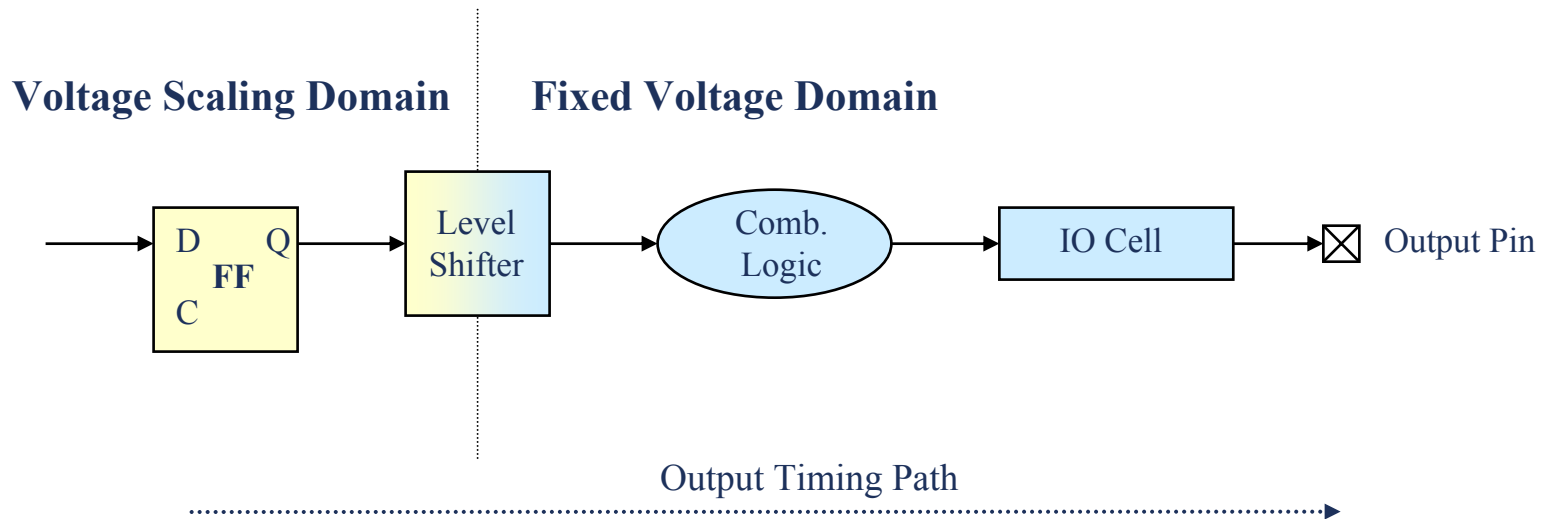
This voltage domain partition gives zero setup/hold time variation over voltage scaling range. The timing path between flop F1 and F2 must be balanced properly to account for the clock skew caused by voltage scaling.

# Output Timing Voltage Scaling Implication – Scenario 1



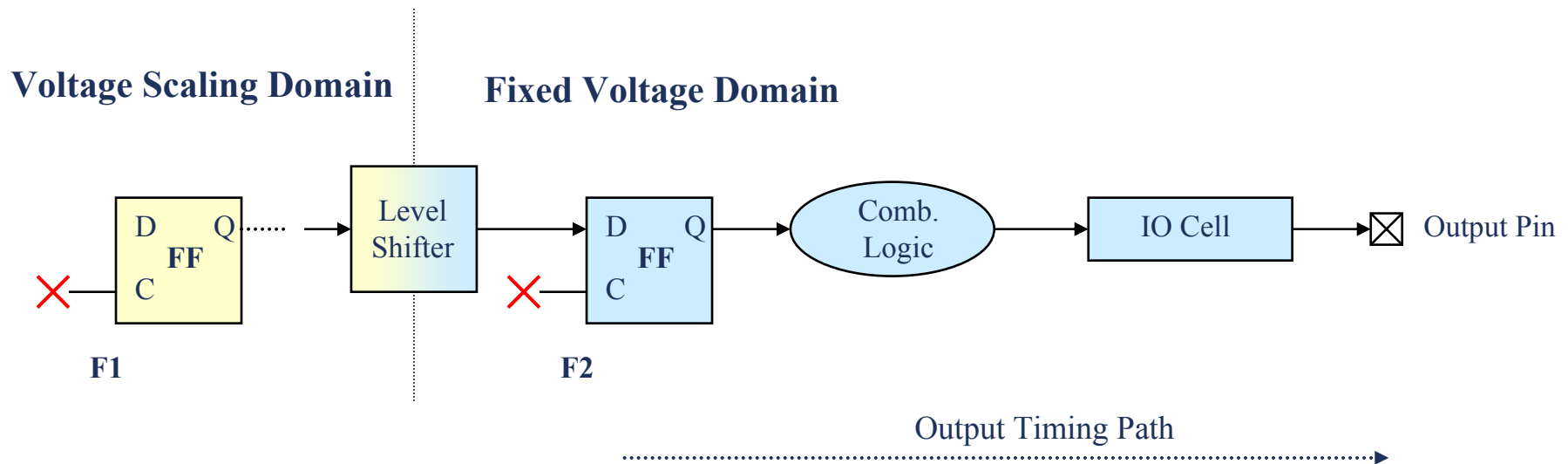
Output timing may vary substantially over voltage scaling range depending on the amount of logic in between output flop and level shifter.

# Output Timing Voltage Scaling Implication – Scenario 2



This voltage domain partition gives smaller output timing variation over voltage scaling range.

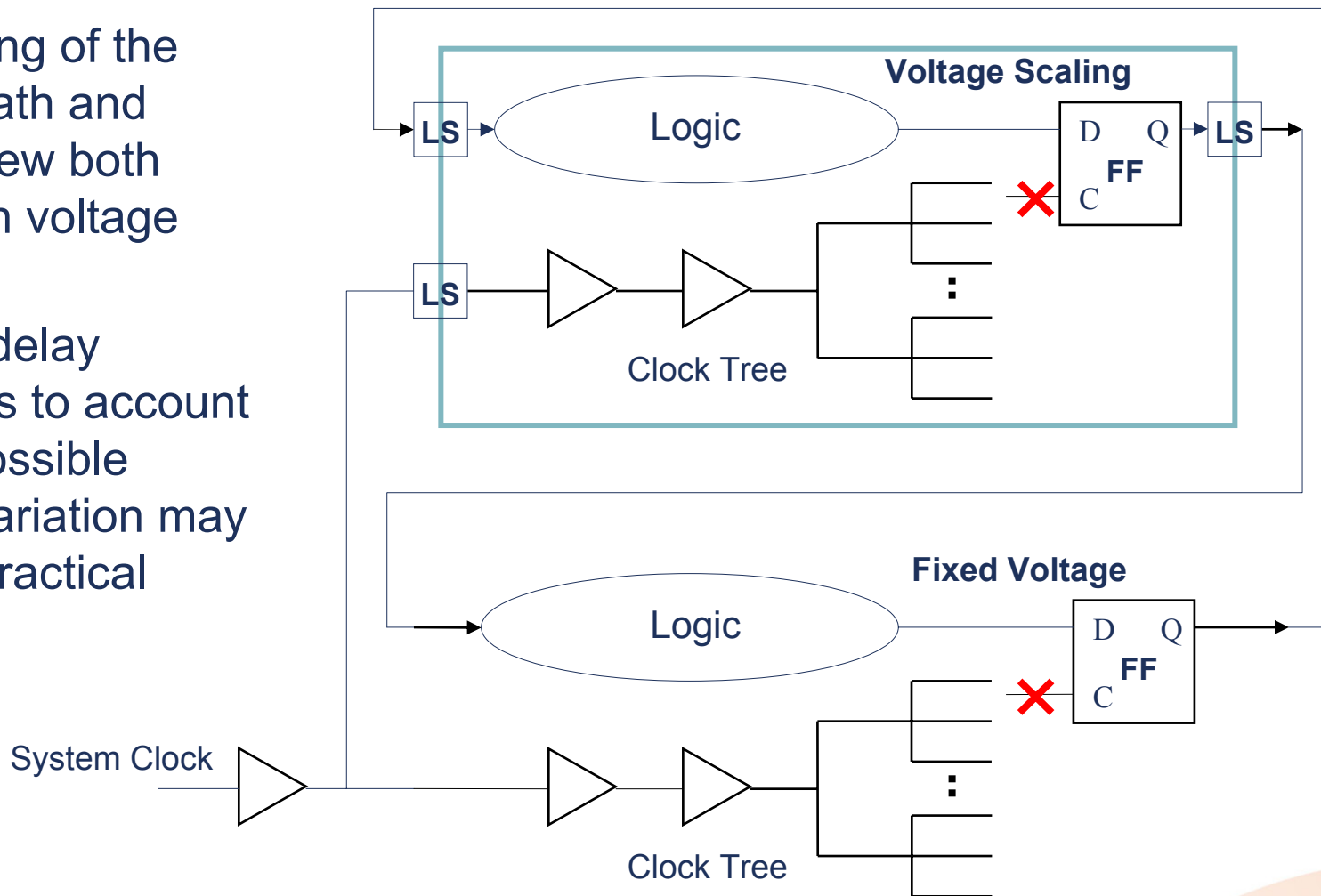
# Output Timing Voltage Scaling Implication – Scenario 3



This voltage domain partition gives zero output timing variation over voltage scaling range. The timing path between flop F1 and F2 must be balanced properly to account for the clock skew caused by voltage scaling.

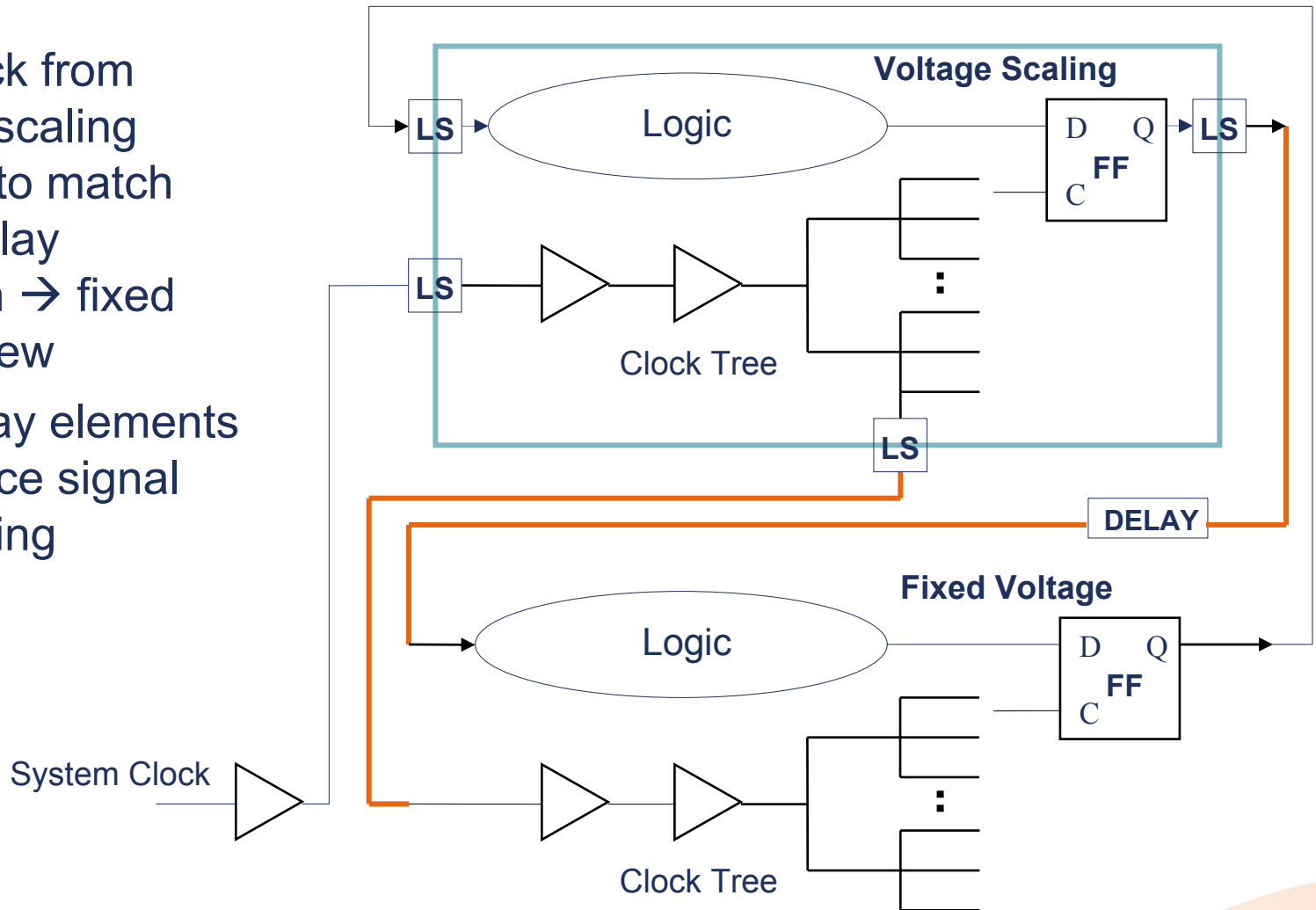
# Synchronous Interface at Voltage Scaling Domain Boundary

- The timing of the signal path and clock skew both vary with voltage level
- Adding delay elements to account for all possible timing variation may not be practical



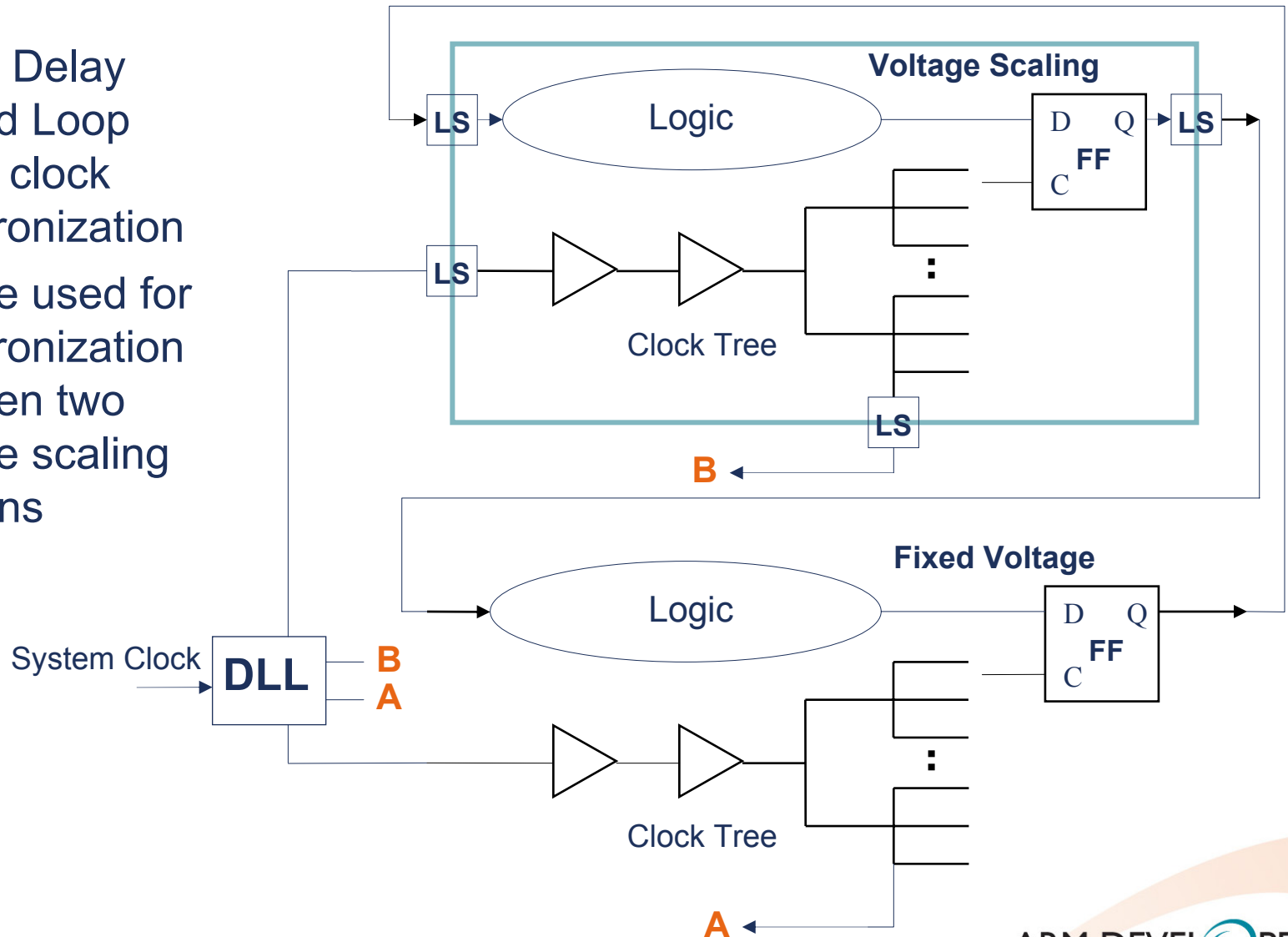
# Pseudo Synchronization at Voltage Scaling Domain Boundary

- Tap clock from voltage scaling domain to match clock delay variation → fixed clock skew
- Add delay elements to balance signal path timing

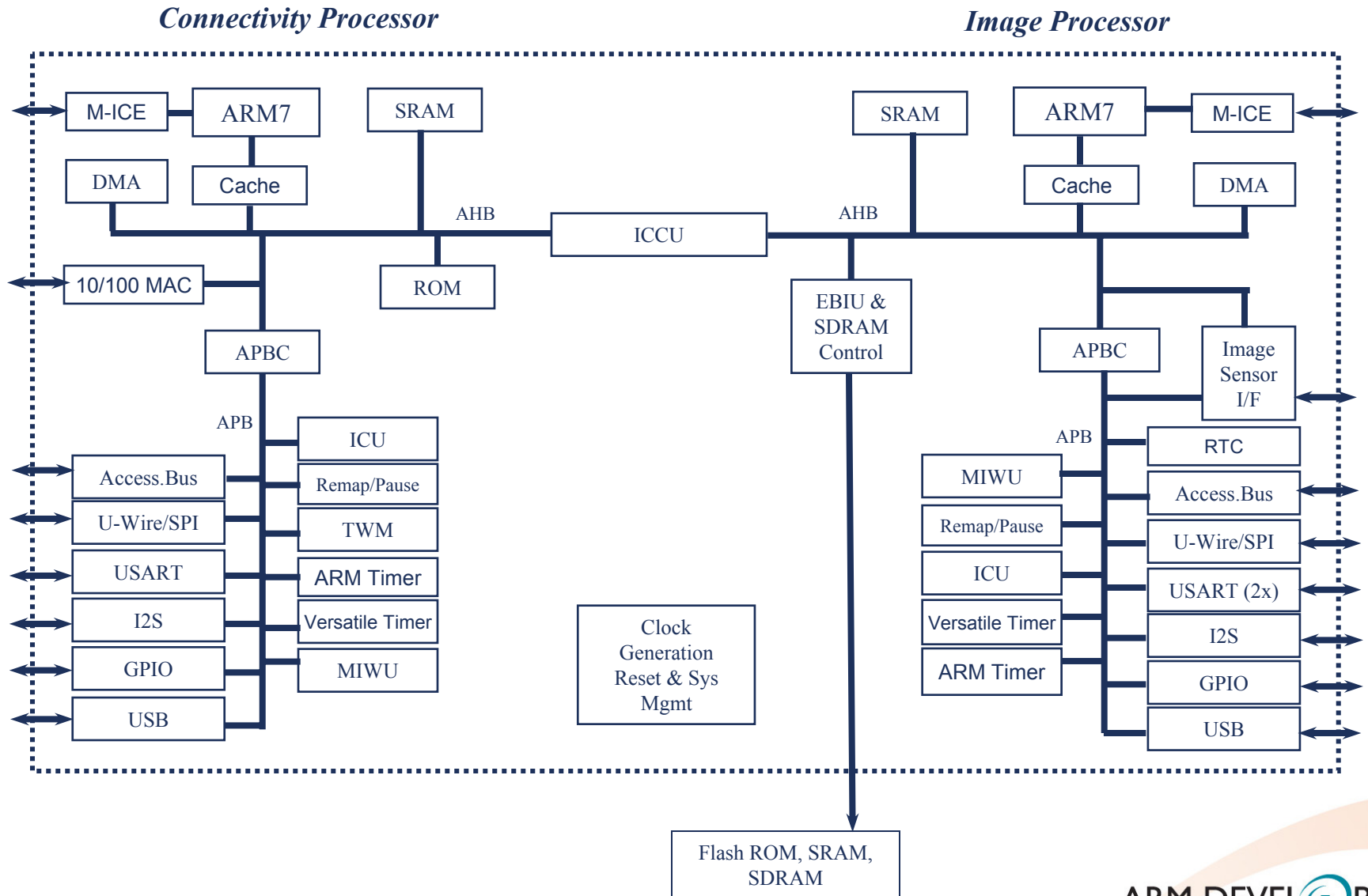


# DLL Synchronization at Voltage Scaling Domain Boundary

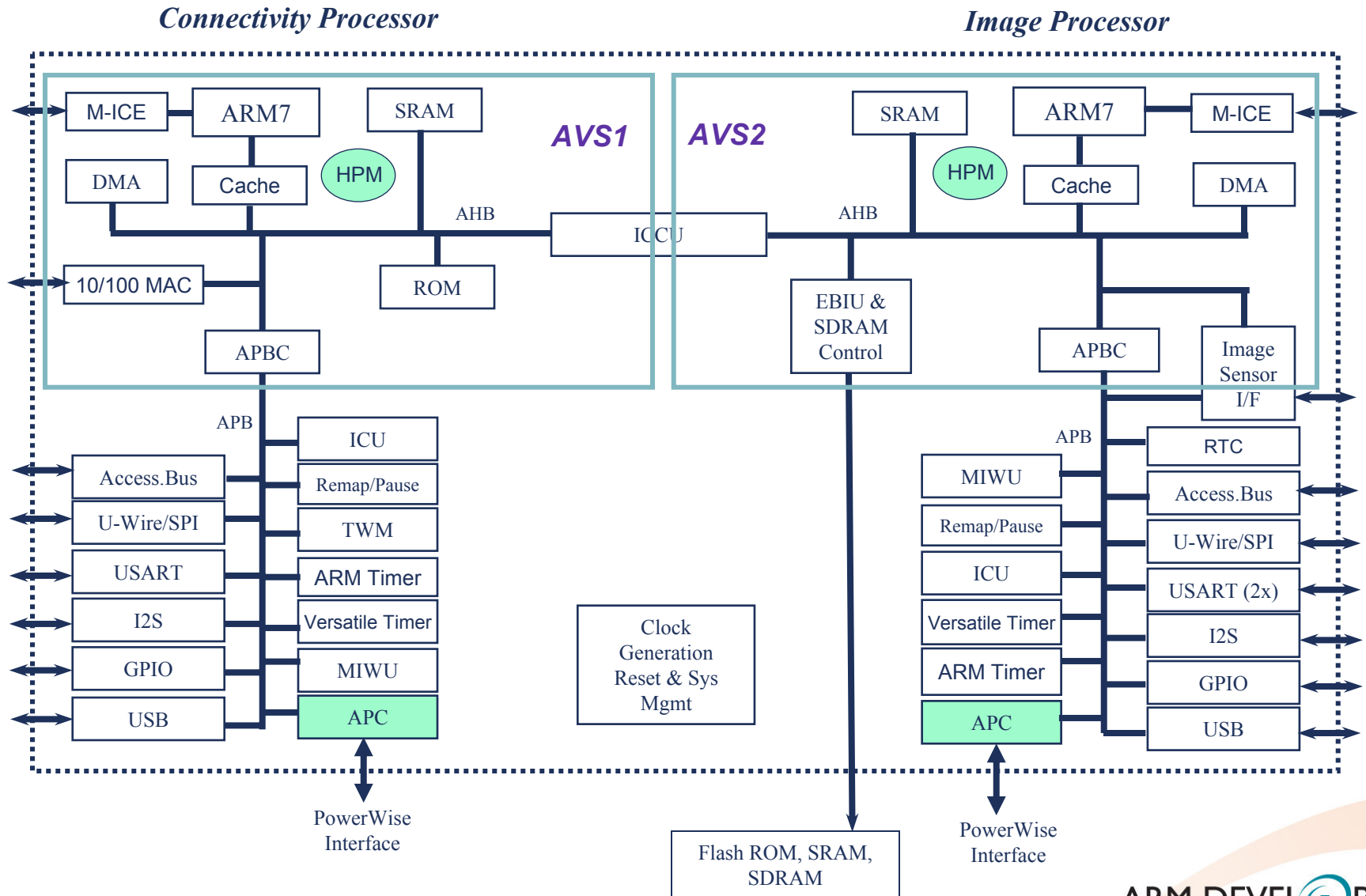
- Digital Delay Locked Loop based clock synchronization
- Can be used for synchronization between two voltage scaling domains



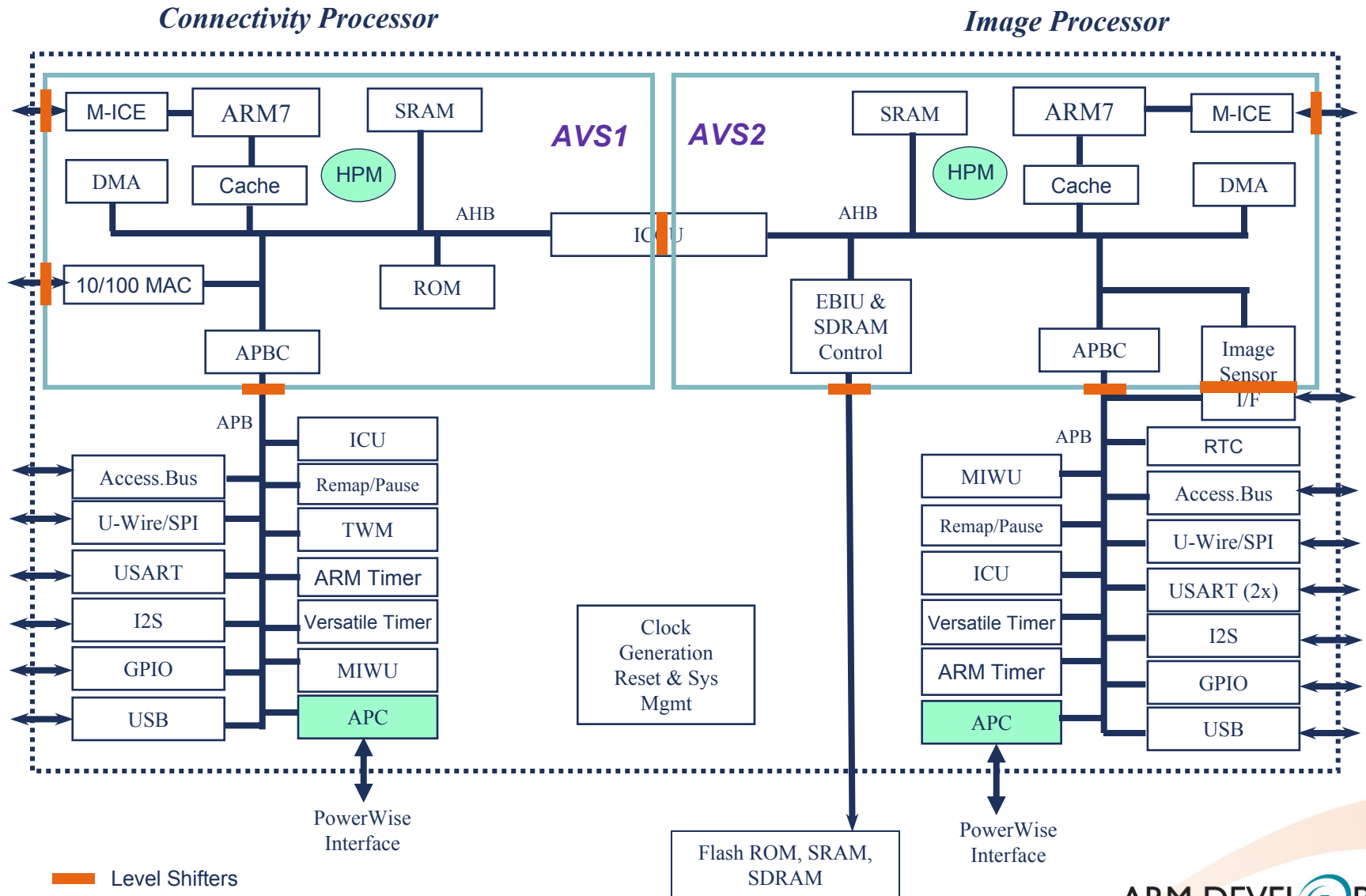
# PowerWise™ Camera – without voltage scaling



# PowerWise™ Camera – added voltage scaling



# PowerWise™ Camera – level shifters inserted



# Early Voltage Domain Considerations in Design Cycle

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- Cell libraries characterized for voltage scaling
- Design hierarchy/partition considerations include voltage domains, level shifters
- Include P/G network in RTL and gate netlist for simulation, level shifter insertion, synthesis, layout, and timing analysis
- Include voltage domains in functional simulation - especially when some voltage domains can be powered off
- Global signals (reset, ...) crossing voltage domain boundary - asynchronous signals only
- Clock tree synthesis should not cross voltage domain boundary
- Scan chain routing should not cross voltage domain boundary
- ECO and buffer insertion should not cross voltage domain boundary
- Power connectivity verification
- and many more .....

# Summary

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- A good design partition based on both functional partition and voltage domain partition will make voltage scaling easier to implement
- Level shifters must be properly inserted and thoroughly verified
- Synchronous timing across voltage scaling domain must be carefully designed and thoroughly checked