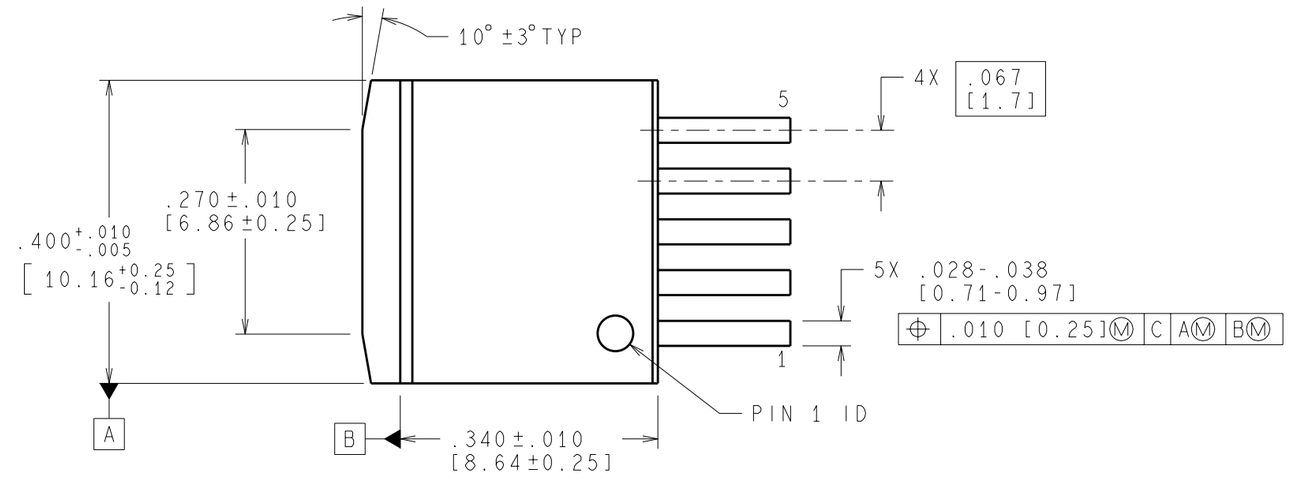
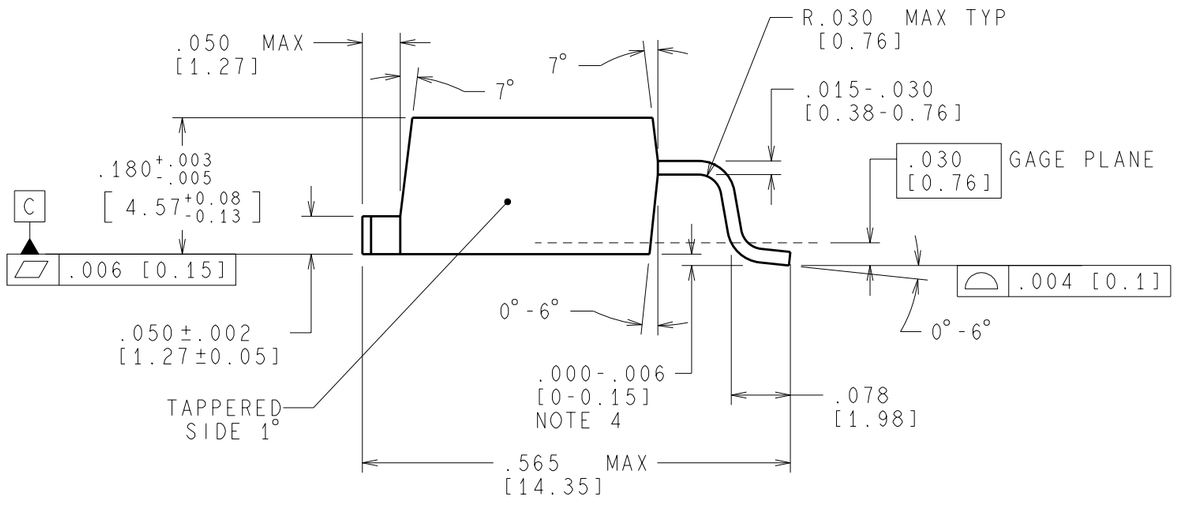
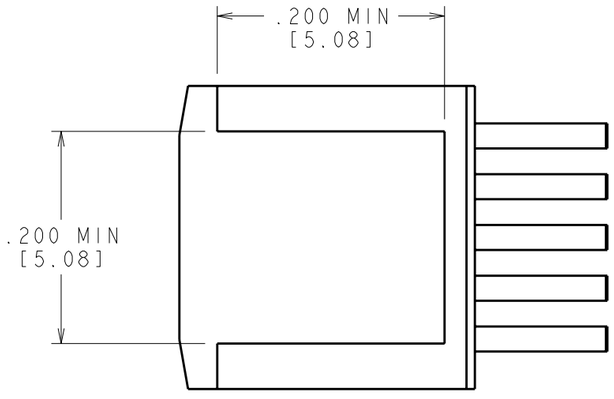
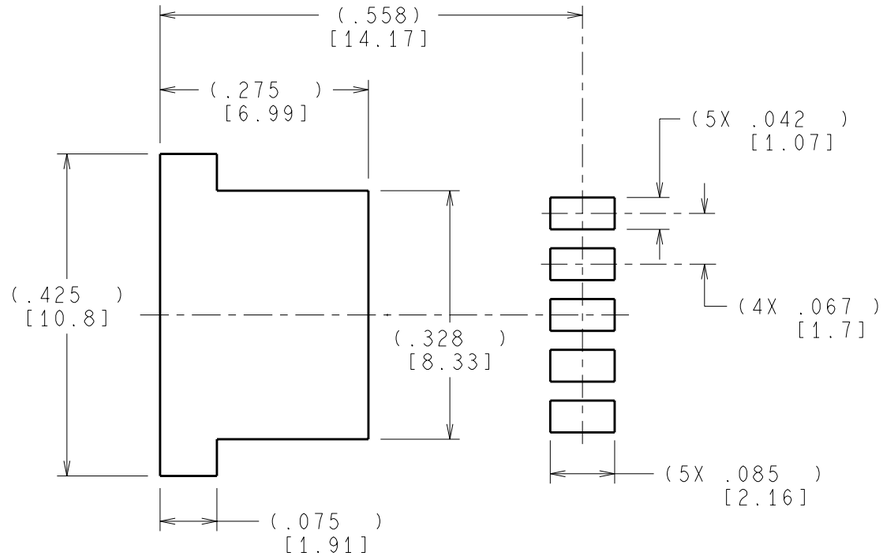
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
D	REVISE & REDRAW PER CURRENT STD ON B SIZE; REVISE LAND PATTERN, TITLE, NOTES 1,4 & 5	1777	04/14/2005	TL/RW









LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM VERTICAL BURR ON HEATSINK NOT TO EXCEED .003 IN/ 0.08 mm.
3. NO PACKAGE CHIPS, CRACKS OR SURFACE INDENTATION ALLOWED AFTER FORMING.
4. UNDER ALL CONDITIONS, LEADS MUST NOT BE ABOVE DATUM C.
5. REFERENCE JEDEC REGISTRATION MO-169, VARIATION AB.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

APPROVALS	DATE
DRAWN T. LEQUANG	04/14/2005
DFTG. CHK. MARTA SUCHY	04/14/2005
ENGR. CHK. RANDALL WALBERG	04/14/2005

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

TO-263, MOLDED, .400x.390x.180in, 5 LD, .067in PITCH, SURF.MOUNT

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-TS5B	D

FORMERLY: N/A — SHEET 1 of 1