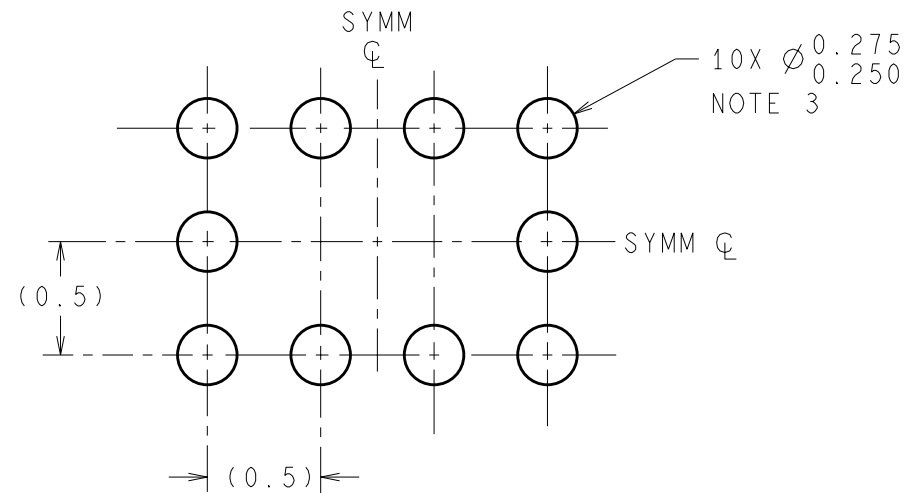
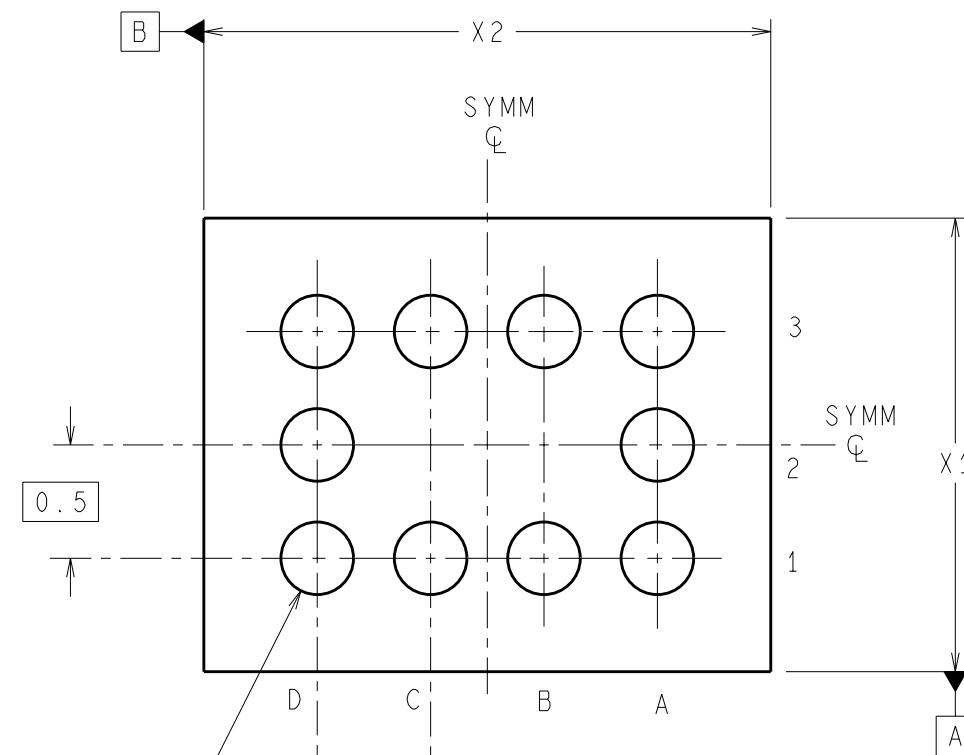
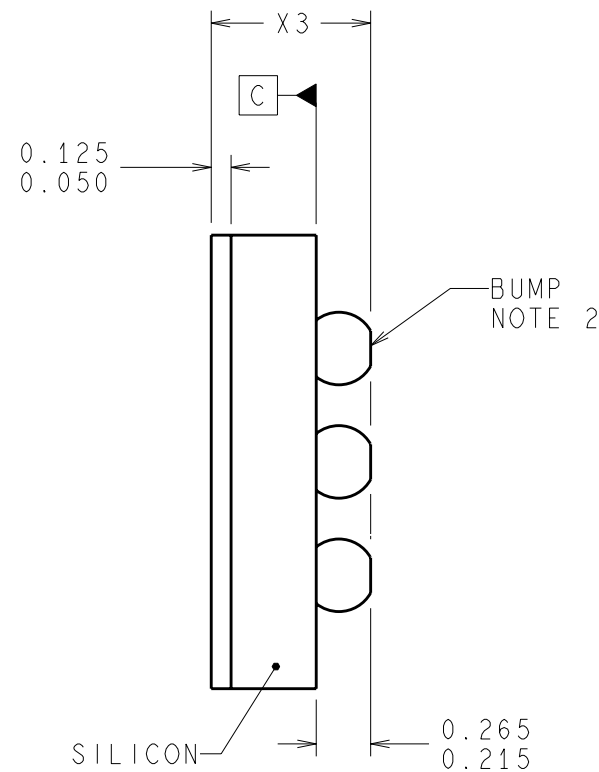
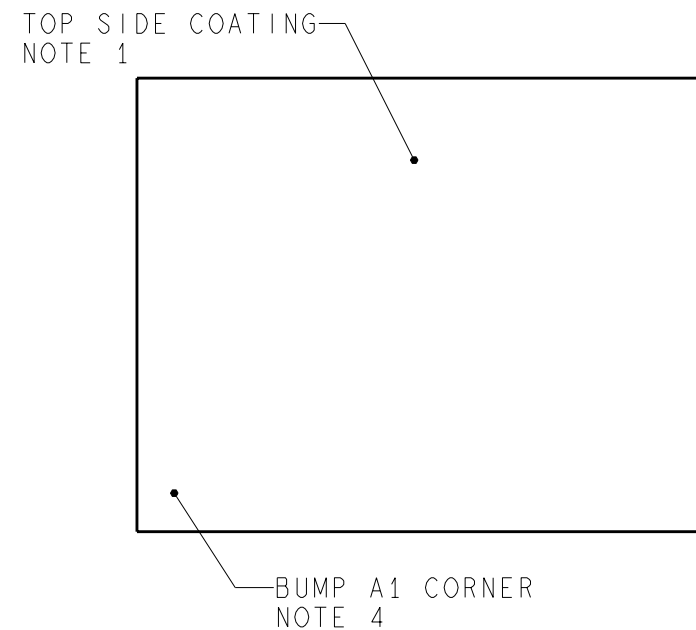


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	566	01/30/2002	MS/VP
B	DIM 0.265/ 0.215 WAS 0.235/ 0.205; DIM 0.125/ 0.050 WAS 0.075/ 0.050; REVISE NOTE 2; ADD 'Z' 1463 & '1' 1488 TO X1 AND 'Z' 1945 & '1' 1970 TO X2 COLUMNS; CHANGE TO B SIZE FORMAT.	856	04/22/2003	MS/HN
C	OPT TBL: REMOVED "Z" & "1" AFTER Y & START 2,3,4 AFTER Y IN COLUMNS X1 & X2.	1152	08/14/2003	MS/VP
D	DIM 0.335/ 0.305 WAS 0.31/ 0.29.	1365	03/10/2004	MS/VP



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



10X Ø 0.335 / 0.305	⊕ 0.005(S)	C	A(S)	B(S)
---------------------	------------	---	------	------


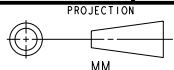
NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING.
2. FOR SOLDER BUMP COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT (SEE TABLE, SHEET 2).
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BD.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	MARTA SUCHY	01/30/2002		
DFTG. CHK.	THANH LEQUANG	03/10/2004	THIN MICRO SMD, 10 BUMP(LARGE), PERIPHERAL, 0.5mm PITCH	
ENGR. CHK.	VIRAJ PATWARDHAN	03/10/2004		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-TLP10XXX	D
FORMERLY: N/A			SHEET 1 of 2	

REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
SEE SHEET 1				

PACKAGE DIMENSIONS					
X1 DESIGNATOR	X1 PACKAGE WIDTH $\pm 30 \mu\text{m}$	X2 DESIGNATOR	X2 PACKAGE LENGTH $\pm 30 \mu\text{m}$	X3 DESIGNATOR	X3 PACKAGE HEIGHT $\pm 75 \mu\text{m}$
Z	1463	Z	1945	A	600
1	1488	1	1970		
A	1514	A	1996		
B	1539	B	2022		
C	1565	C	2047		
D	1590	D	2073		
E	1615	E	2098		
F	1641	F	2123		
G	1666	G	2149		
H	1692	H	2174		
J	1717	J	2200		
K	1742	K	2225		
L	1768	L	2250		
M	1793	M	2276		
N	1819	N	2301		
P	1844	P	2327		
Q	1869	Q	2352		
R	1895	R	2377		
S	1920	S	2403		
T	1946	T	2428		
U	1971	U	2454		
V	1996	V	2479		
W	2022	W	2504		
X	2047	X	2530		
Y	2073	Y	2555		
2	2098	2	2581		
3	2123	3	2606		
4	2149	4	2631		
5	2174	5	2657		
6	2200	6	2682		
7	2225	7	2708		
8	2250	8	2733		

APPROVALS	DATE	 National Semiconductor <small>2900 Semiconductor Dr., Santa Clara, CA 95052-8090</small>
DRAWN MARTA SUCHY	01/30/2002	
DFTG. CHK. THANH LEQUANG	03/10/2004	
ENGR. CHK. VIRAJ PATWARDHAN	03/10/2004	
 PROJECTION MM		THIN MICRO SMD, 10 BUMP(LARGE), PERIPHERAL, 0.5mm PITCH
SCALE NTS	SIZE B	DRAWING NUMBER (SC)MKT-TLP10XXX
FORMERLY: N/A		REV D SHEET 2 of 2