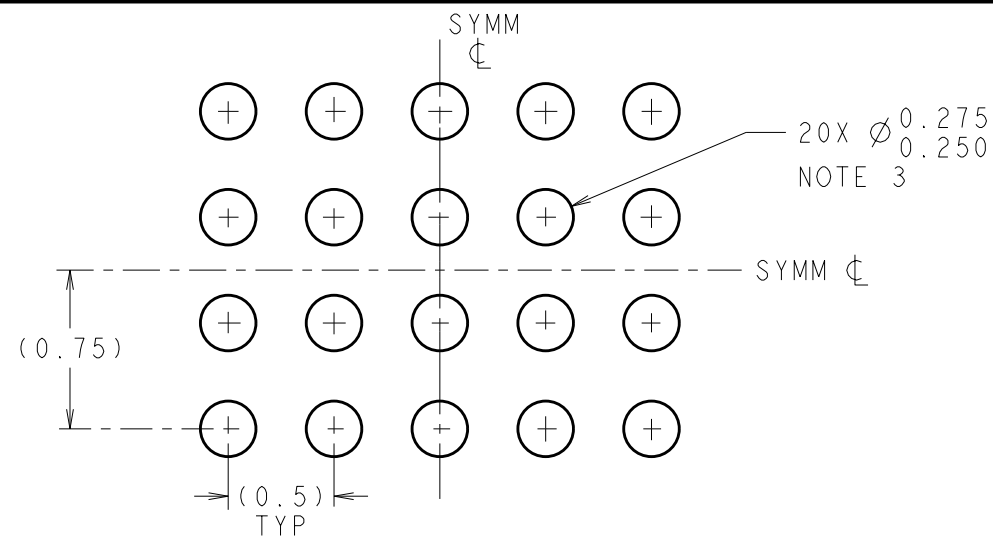


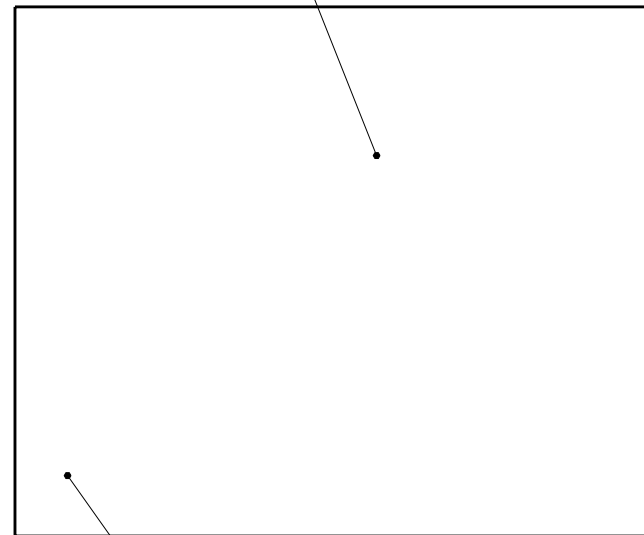
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	589	02/26/2002	MS/VA
B	DIM 0.265/ 0.215 WAS 0.235/ 0.205; DIM 0.125/ 0.050 WAS 0.075/ 0.050; REVISE NOTE 2; ADD 'Z' 1945 & '1' 1970 TO X1 AND 'Z' 2441 & '1' 2466 TO X2 COLUMNS.	852	05/02/2003	MS/HN
C	BUMP DIA 0.335/ 0.305 WAS 0.31/ 0.29	1292	01/21/2004	MS/HN
D	ADD V & W DESIGNATORS & THEIR VALUES TO X1 & X2 COLUMNS.	2133	07/26/2006	MS/VP



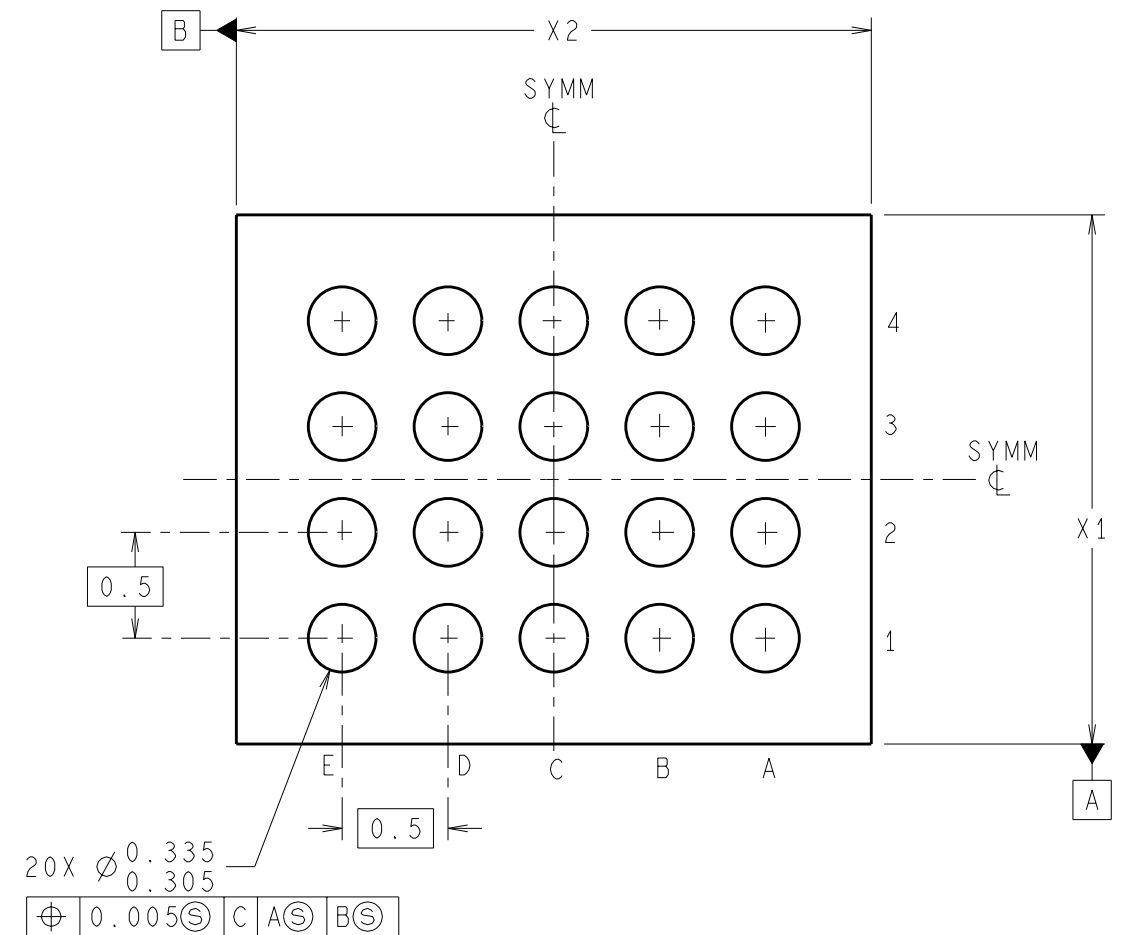
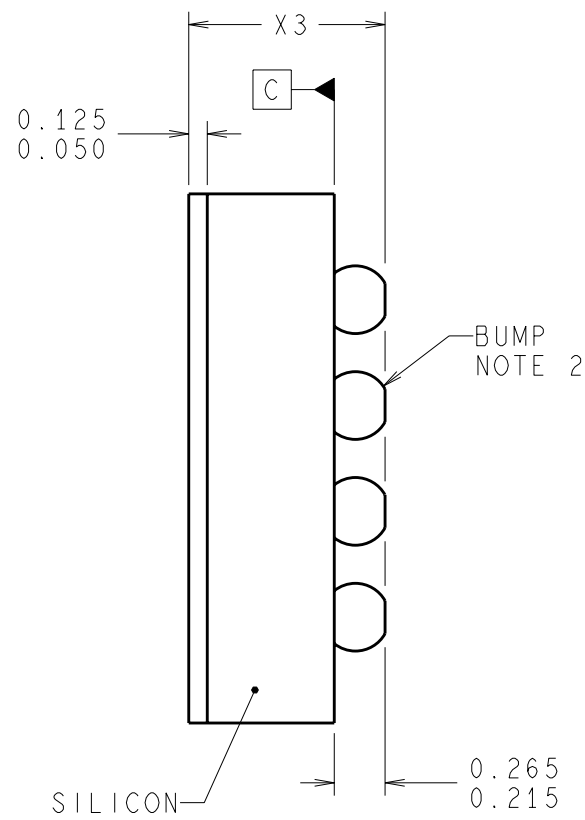
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION

TOP SIDE COATING
NOTE 1



BUMP A1 CORNER
NOTE 4





NOTES: UNLESS OTHERWISE SPECIFIED

- EPOXY COATING.
- FOR SOLDER BUMP COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
- PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
- XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT (SEE TABLE, SHEET 2).
- REFERENCE JEDEC REGISTRATION MO-211, VARIATION DG.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN	MARTA SUCHY	02/26/2002	
DFTG. CHK.	KURT SINCERBOX	07/26/2006	
ENGR. CHK.	VIRAJ PATWARDHAN	07/26/2006	
THIN MICRO SMD, 20 BUMP(LARGE), 0.5mm PITCH			SCALE: NTS SIZE: B DRAWING NUMBER: (SC)MKT-TLA20XXX REV: D
PROJECTION: MM			
FORMERLY: N/A			SHEET 1 of 2

REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	SEE SHEET 1			

PACKAGE DIMENSIONS (MICROMETERS)					
X1 DESIGNATOR	X1 PACKAGE WIDTH $\pm 30\mu\text{m}$	X2 DESIGNATOR	X2 PACKAGE LENGTH $\pm 30\mu\text{m}$	X3 DESIGNATOR	X3 PACKAGE HEIGHT $\pm 75\mu\text{m}$
Z	1945	Z	2441	A	600
1	1970	1	2466		
A	1996	A	2492		
B	2022	B	2517		
C	2047	C	2543		
D	2073	D	2568		
E	2098	E	2593		
F	2123	F	2619		
G	2149	G	2644		
H	2174	H	2670		
J	2200	J	2695		
K	2225	K	2720		
L	2250	L	2746		
M	2276	M	2771		
N	2301	N	2797		
P	2327	P	2822		
Q	2352	Q	2847		
R	2377	R	2873		
S	2403	S	2898		
T	2428	T	2924		
U	2454	U	2949		
V	2479	V	2974		
W	2505	W	3000		

APPROVALS		DATE	 National Semiconductor <small>2900 Semiconductor Dr., Santa Clara, CA 95052-8090</small>		
DRAWN	MARTA SUCHY	02/26/2002			
DFTG. CHK.	KURT SINCERBOX	07/26/2006			
ENGR. CHK.	VIRAJ PATWARDHAN	07/26/2006			
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
 MM		NTS	B	(SC)MKT-TLA20XXX	D
FORMERLY: N/A		SHEET 2 of 2			