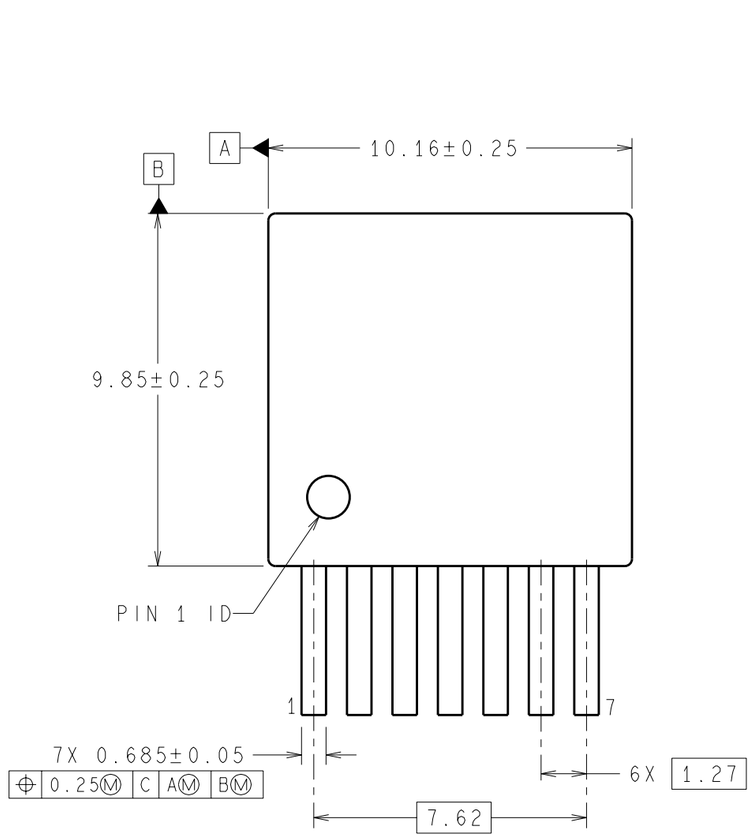
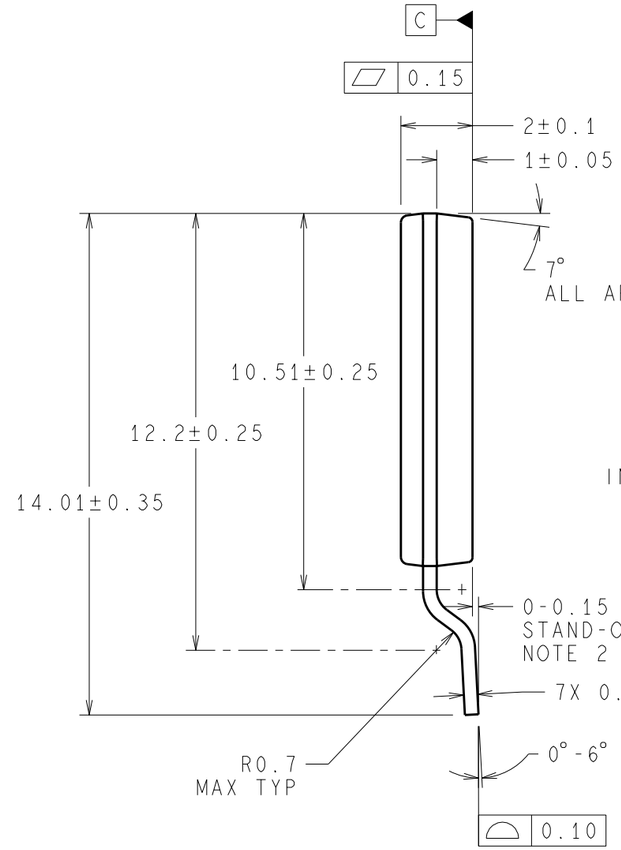
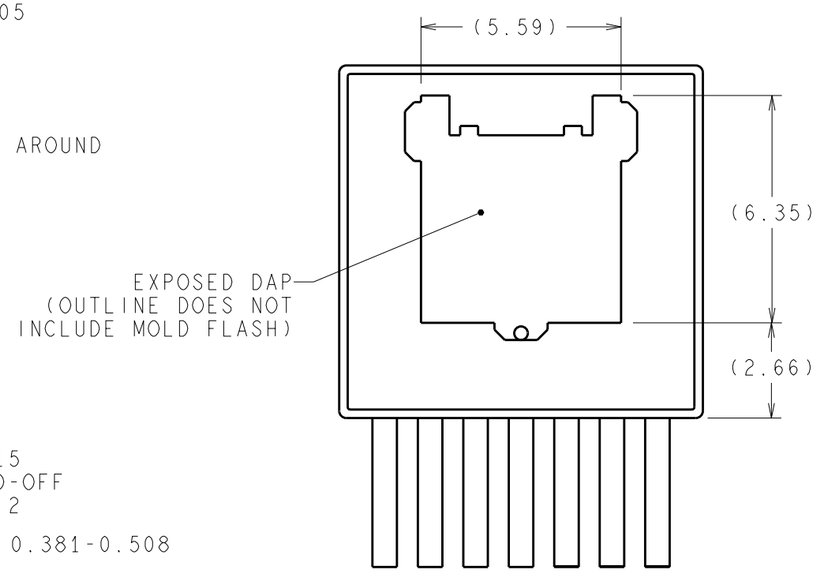
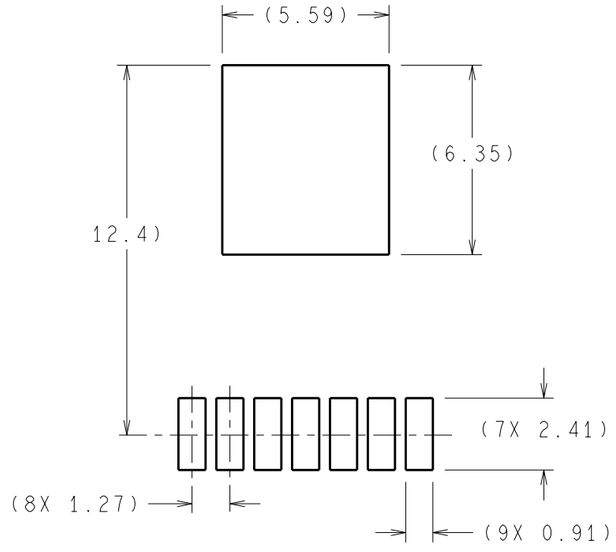
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2063	03/20/2006	AS/MS/AS
B	UPDATE EXPOSED DAP; UPDATE NOTE 3	2394	09/20/2007	EL/TL/EL
C	UPDATE NOTE 3; ADD "OUTLINE DOES NOT INCLUDE MOLD FLASH" UNDER EXPOSED DAP	2454	01/02/2008	EL/TL/EL







DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. UNDER ALL CONDITIONS, LEADS MUST NOT BE ABOVE DATUM C.
3. NO JEDEC REGISTRATION AS OF JANUARY 2008.

APPROVALS	DATE
DRAWN ASNOR SULAIMAN	03/20/2006
DFTG. CHK. THANH LEQUANG	01/02/2008
ENGR. CHK. EUGENE LEE	01/02/2008

National Semiconductor
2900 Semiconductor Dr, Santa Clara, CA 95052-8090

THIN TO-263, MOLDED,
9.85x10.16X2.0mm,
7 LD, 1.27mm PITCH, SMT

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
MM	NTS	B	(SC)MKT-TJ7A	C

FORMERLY: N/A — SHEET 1 of 1