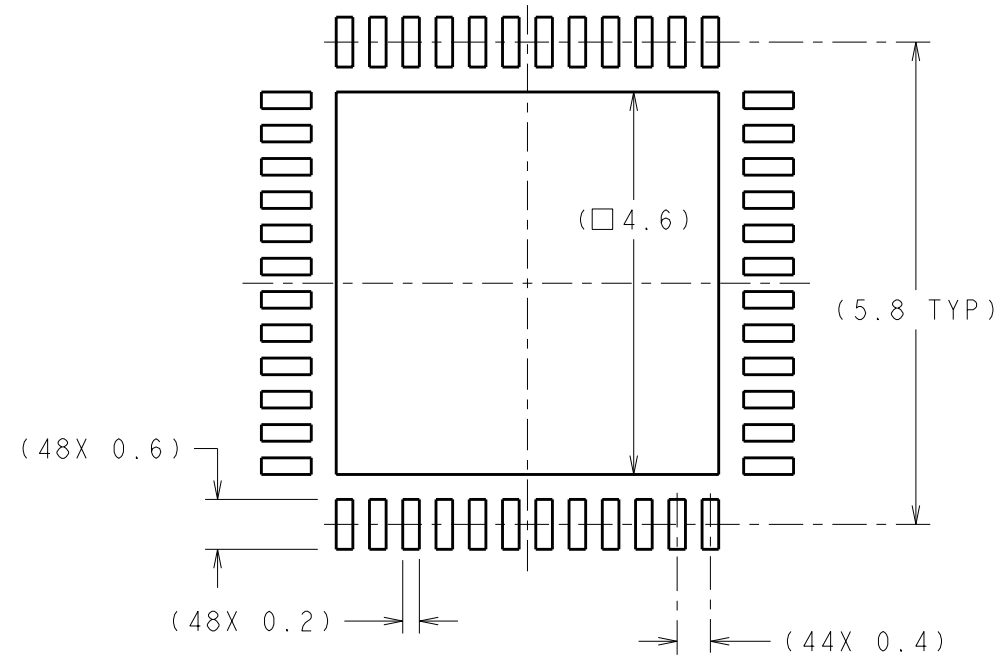
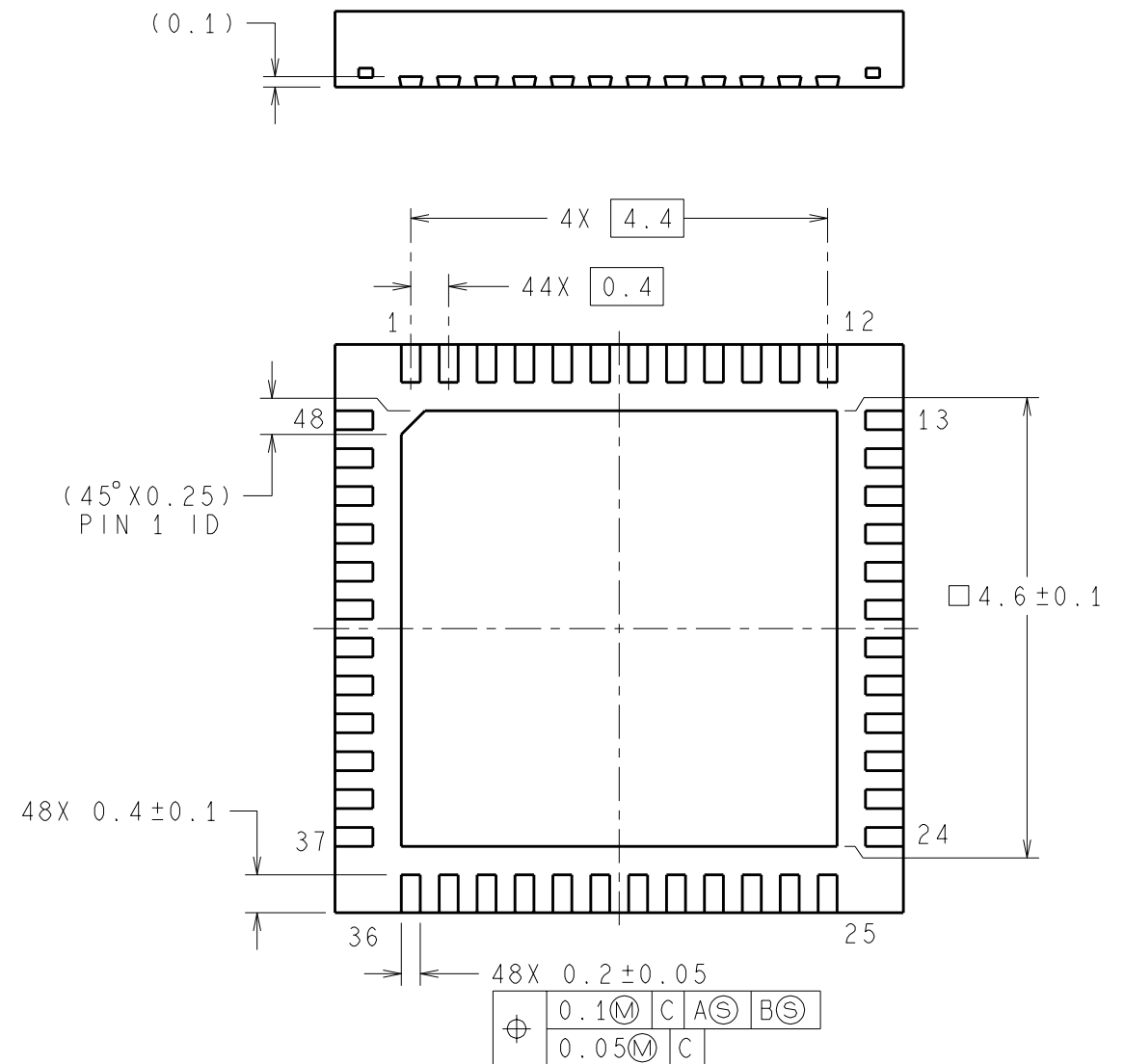
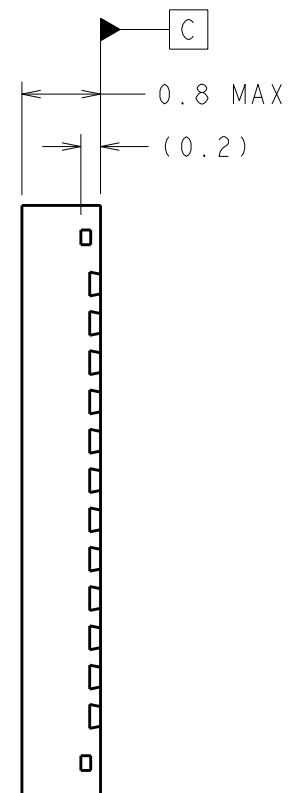
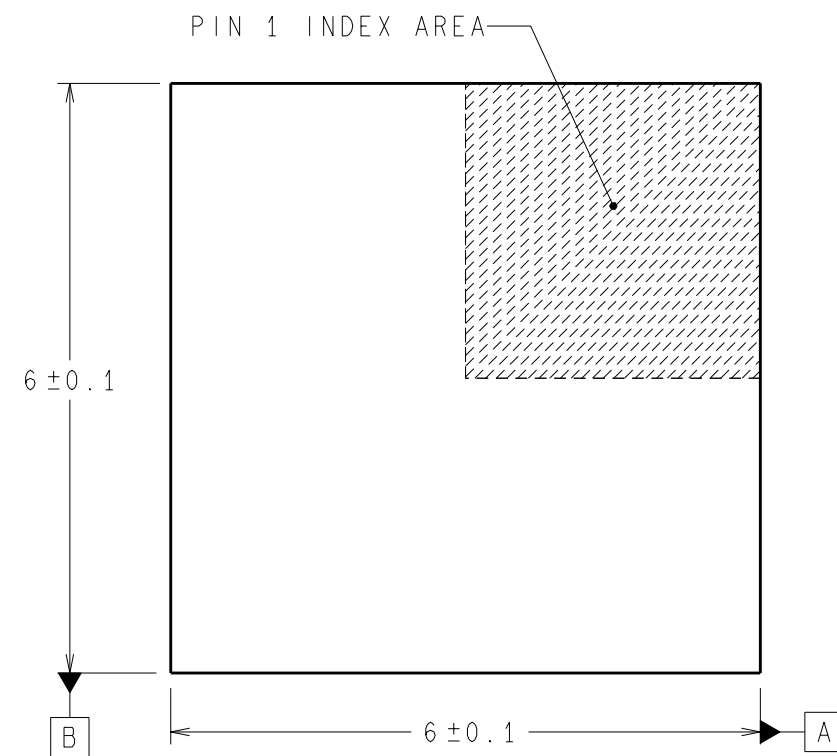


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1465	05/03/2004	TL/JS



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



⊕	0.1(M)	C	A(S)	B(S)
	0.05(M)	C		

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF MAY 2004.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN	T. LEQUANG	05/03/2004	
DFTG. CHK.	MARTA SUCHY	05/03/2004	
ENGR. CHK.	JEFF SCHAEFER	05/03/2004	
PROJECTION:			SCALE: NTS SIZE: B DRAWING NUMBER: (SC)MKT-SQF48A REV: A
FORMERLY: X-01980			SHEET 1 of 1