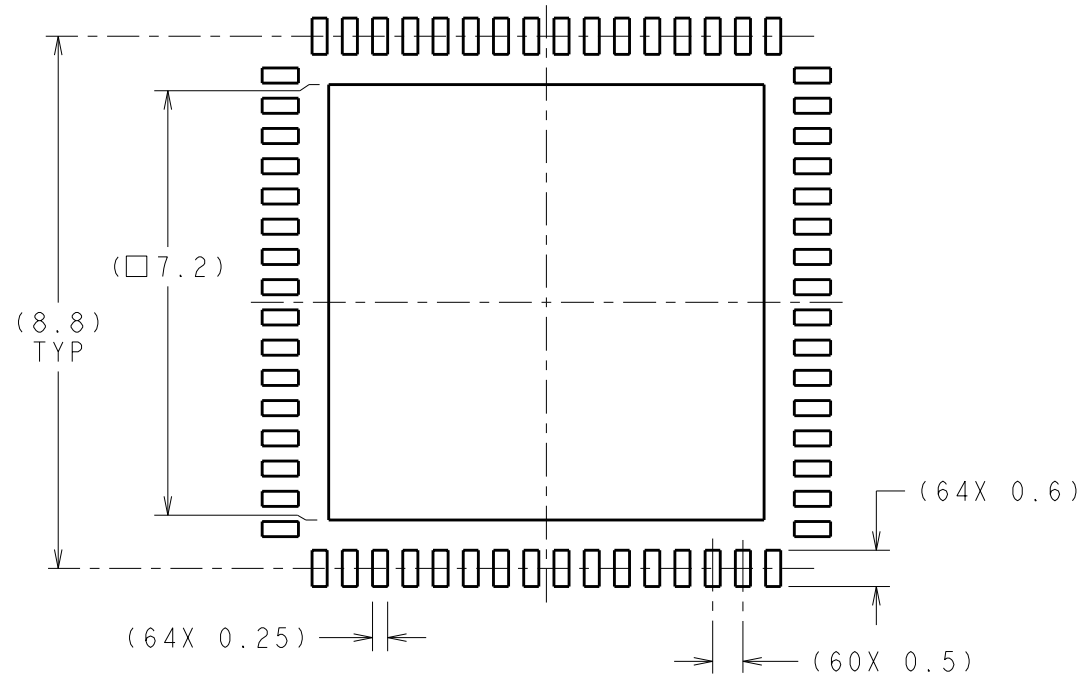
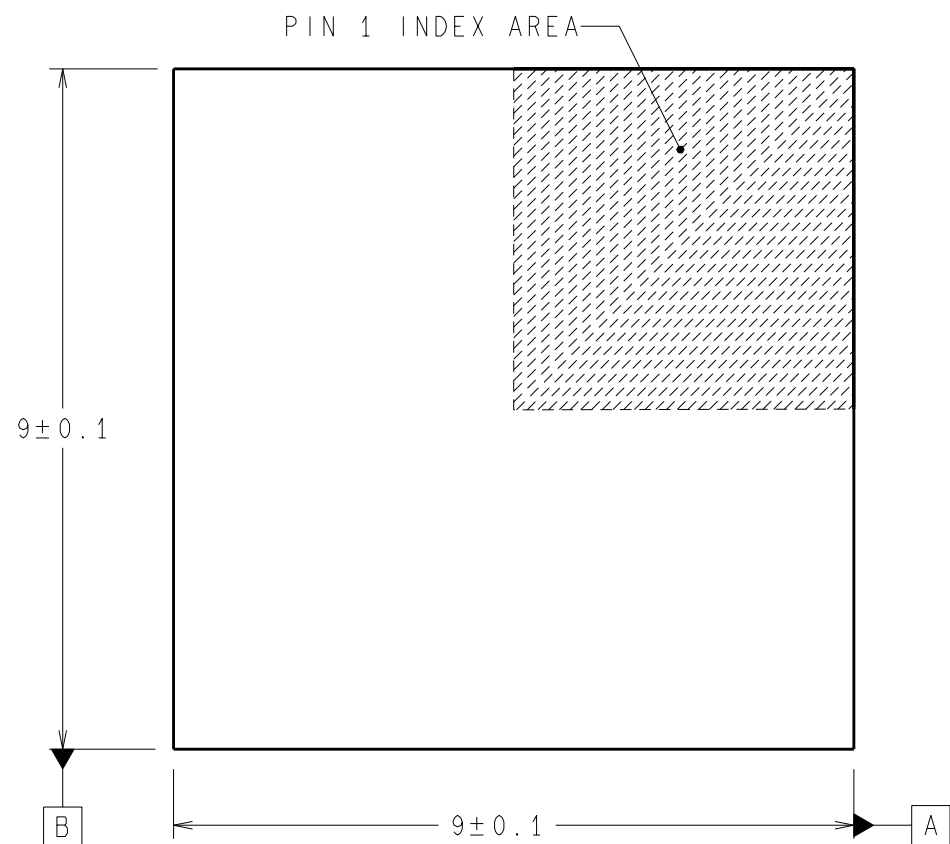


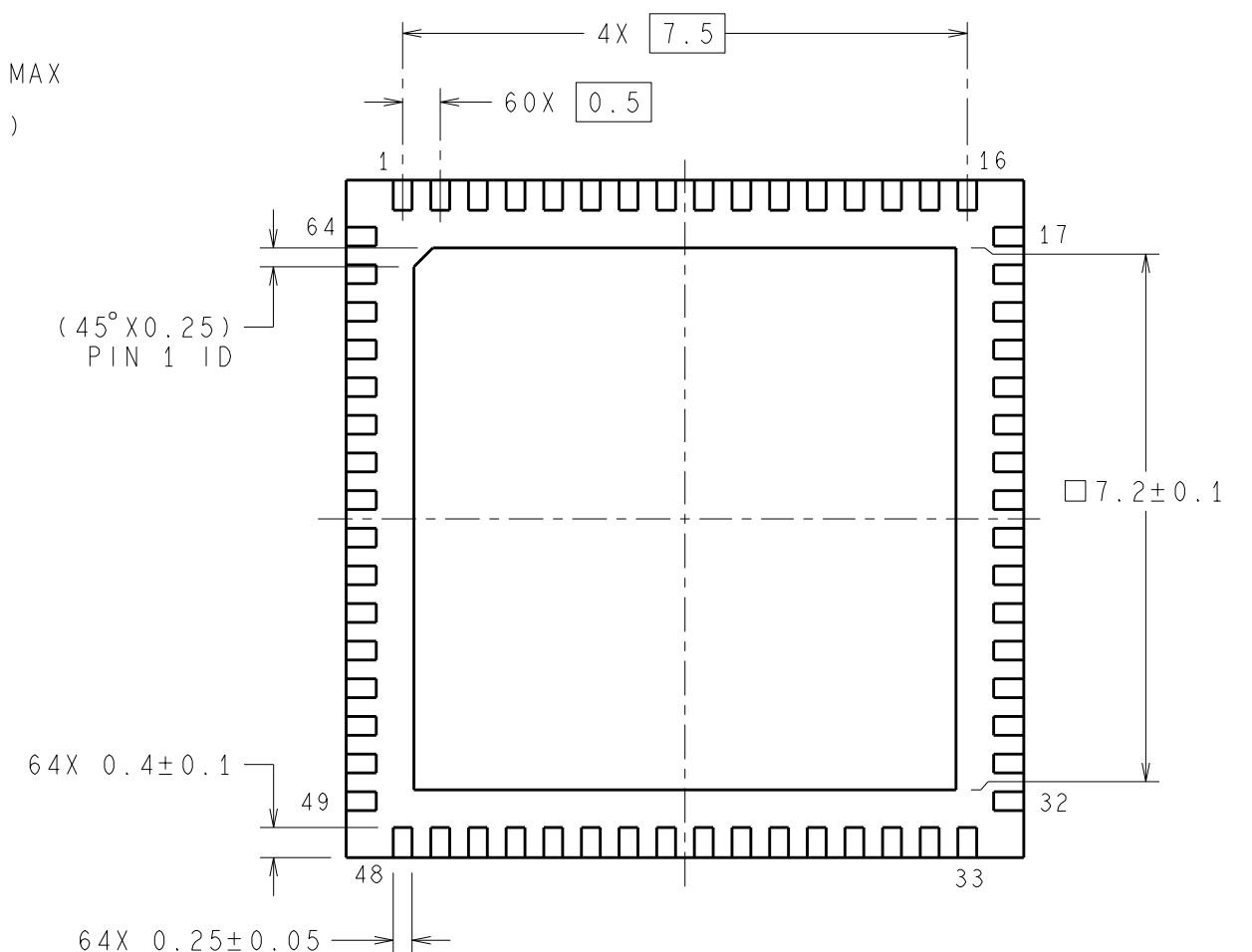
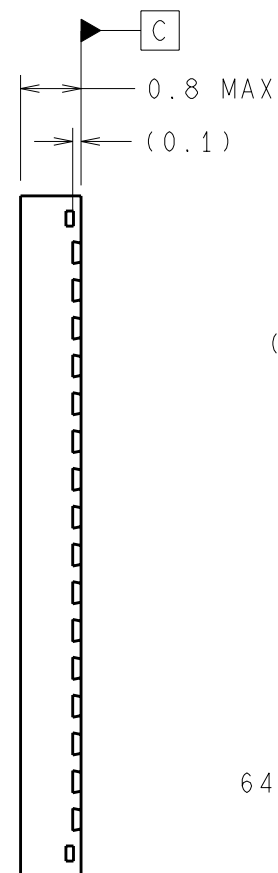
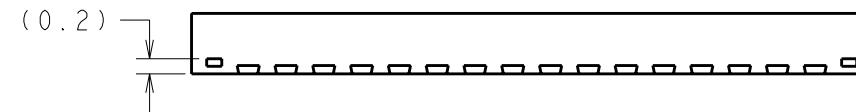
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		2072 04/28/2006	AS/TL/AS



**RECOMMENDED LAND PATTERN**



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



⊕	0.1(M)	C	A(S)	B(S)
	0.05(M)	C		

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE ([www.national.com](http://www.national.com)).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF APRIL 2006.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	<b>LLP, QUAD, 9x9x0.8mm, 64 LD, 0.5mm PITCH, NO LEAD PULLBACK</b>
DRAWN	ASNOR SULAIMAN	04/28/2006		
DFTG. CHK.	THANH LEQUANG	04/28/2006		
ENGR. CHK.	ASNOR SULAIMAN	04/28/2006		
PROJECTION	MM		SCALE	SIZE
			NTS	B
			DRAWING NUMBER	REV
			(SC)MKT-SQA64A	A
			FORMERLY: N/A	SHEET 1 of 1