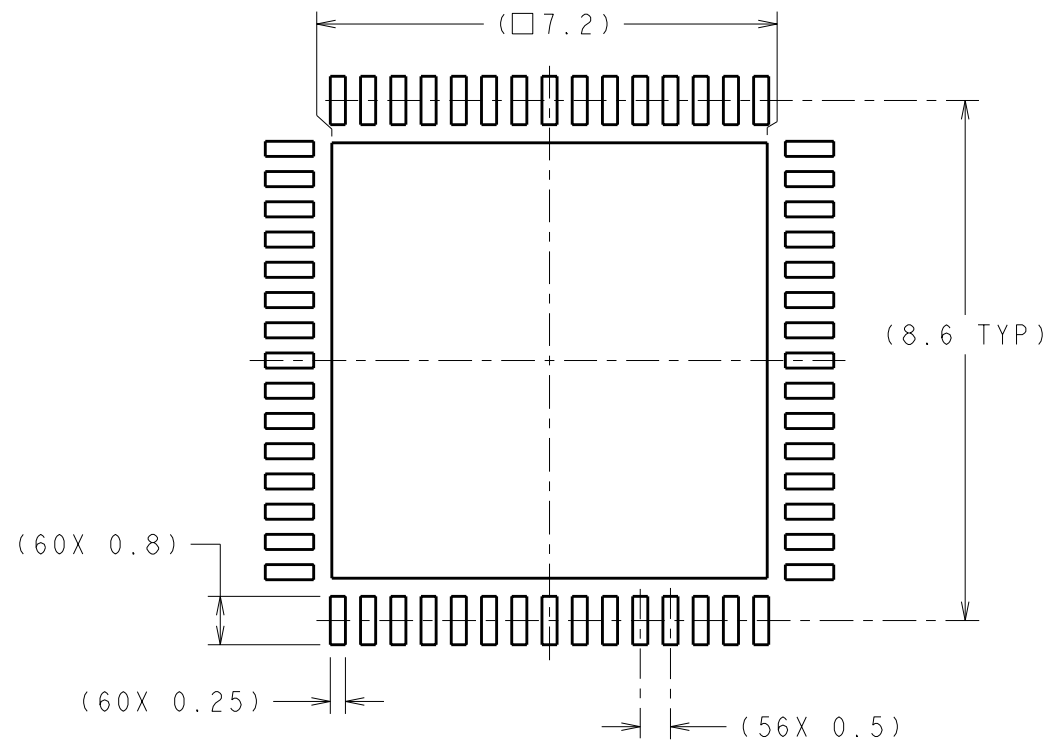
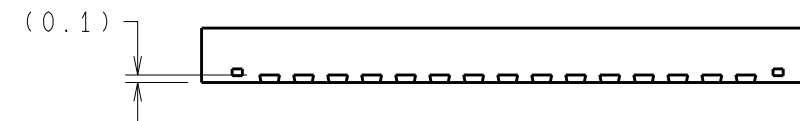


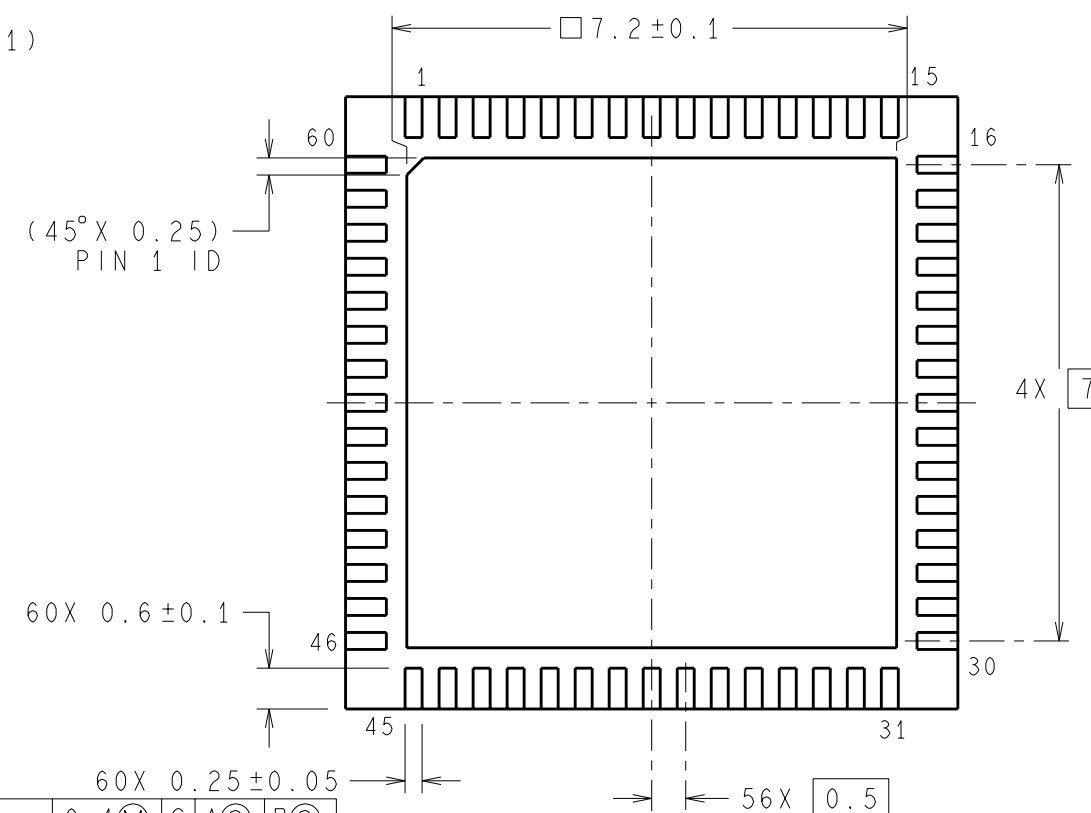
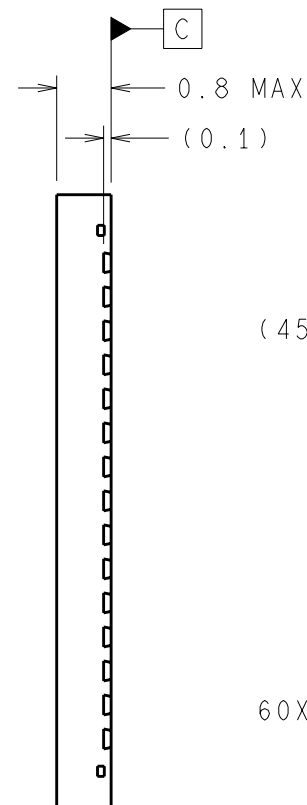
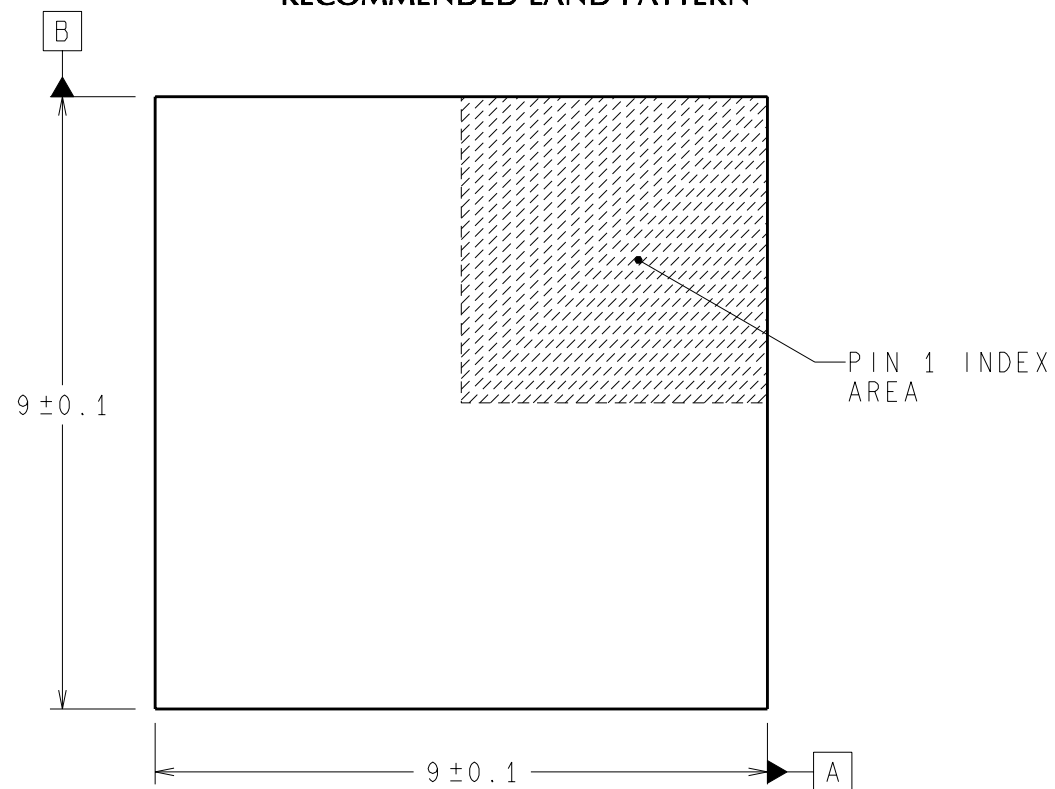
| REVISIONS | | | | |
|-----------|-----------------------------|--------|------------|----------|
| REV | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| A | RELEASE TO DOCUMENT CONTROL | 1854 | 06/29/2005 | AS/TL/SN |



DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



| | | | | |
|---|----------|---|-------|-------|
| ⊕ | 0.1 (M) | C | A (S) | B (S) |
| | 0.05 (M) | C | | |

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF JUNE 2005.

| APPROVALS | | DATE | National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090 |
|---------------|----------------|----------------|----------------------------------------------------------------------------------|
| DRAWN | ASNOR SULAIMAN | 06/29/2005 | |
| DFTG. CHK. | THANH LEQUANG | 06/29/2005 | |
| ENGR. CHK. | ASNOR SULAIMAN | 06/29/2005 | |
| PROJECTION: | | | LLP, QUAD, 9x9x0.8mm, 60 LD, 0.5mm PITCH, NO PULLBACK |
| SCALE | SIZE | DRAWING NUMBER | |
| NTS | B | (SC)MKT-SQA60A | REV A |
| FORMERLY: N/A | | | SHEET 1 of 1 |