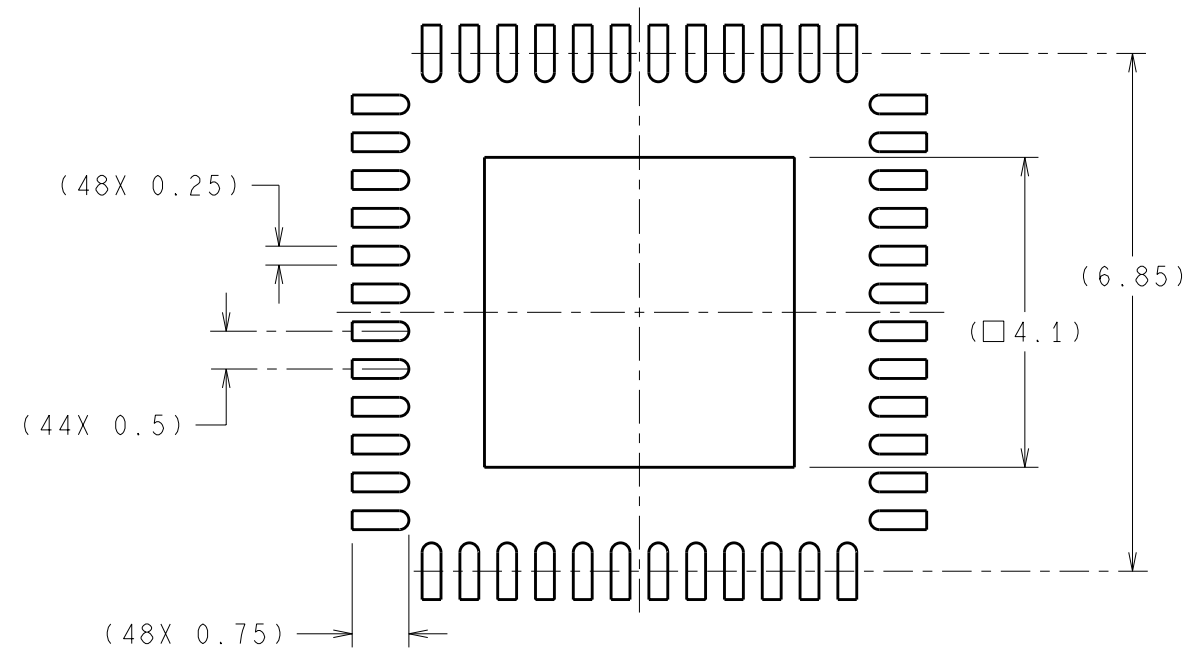
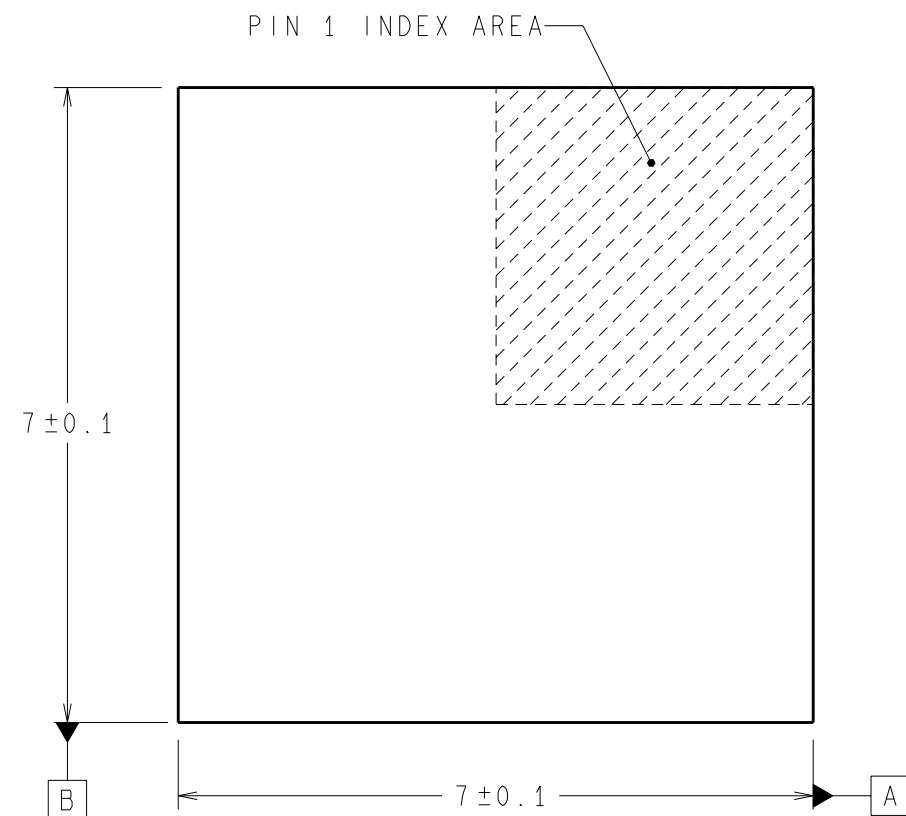


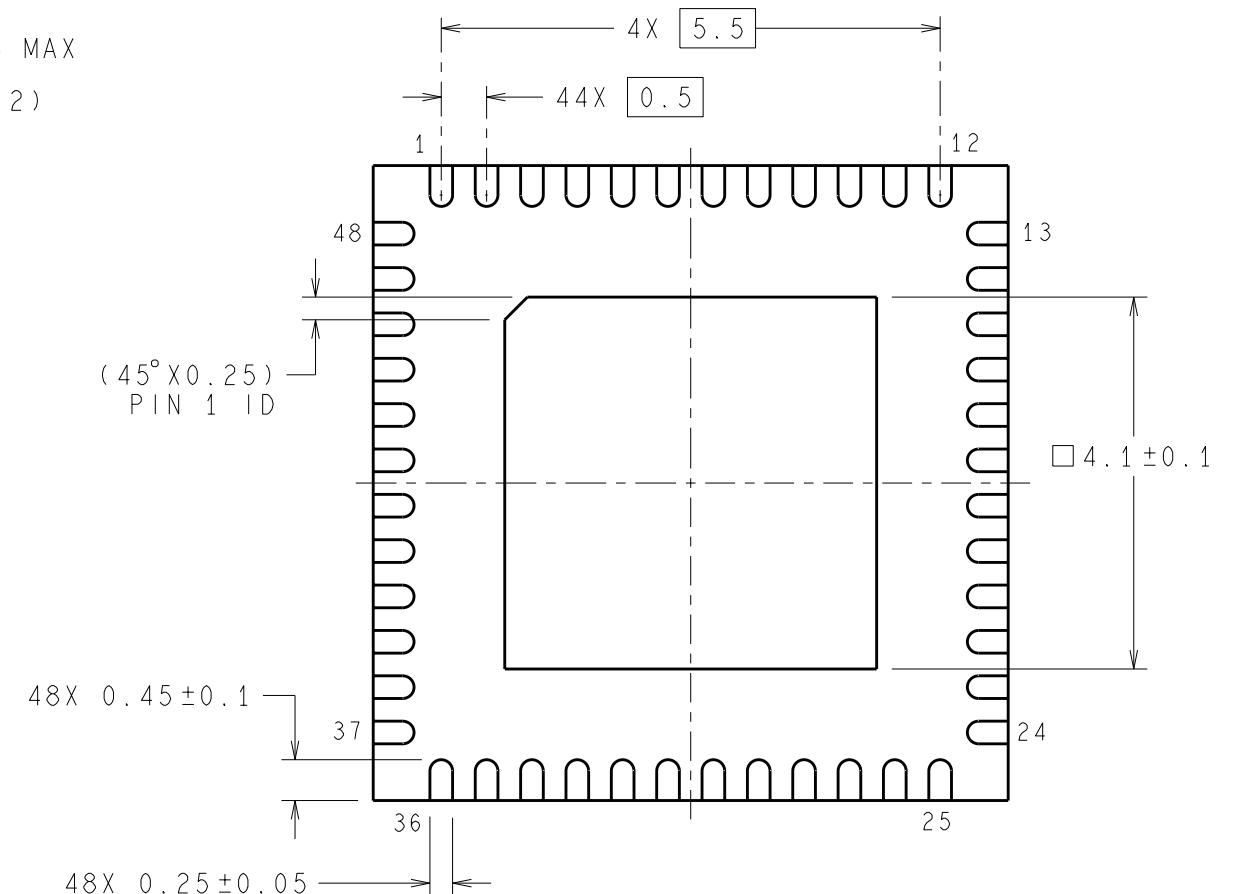
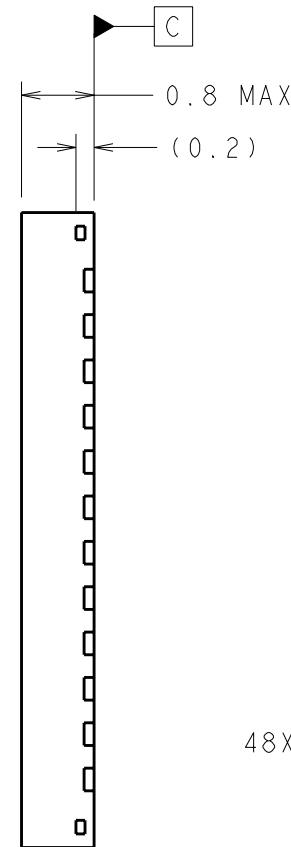
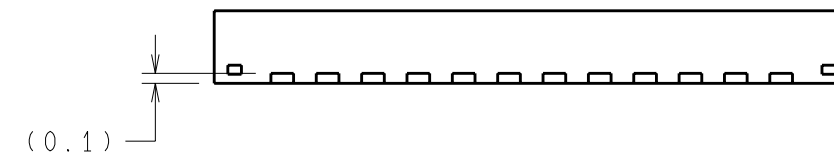
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1525	07/28/2004	TL/HCSL



**RECOMMENDED LAND PATTERN**



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



⊕	0.1 (M)	C	A (S)	B (S)
	0.05 (M)	C		

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE ([www.national.com](http://www.national.com)).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF JULY 2004.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN	T. LEQUANG	07/28/2004	
DFTG. CHK.	MARTA SUCHY	07/28/2004	<b>LLP, QUAD, 7x7x0.8mm, 48 LD, 0.5mm PITCH, 4.1x4.1mm EXP PAD</b>
ENGR. CHK.	HENRY CS LIM	07/28/2004	
PROJECTION  MM			SCALE <b>NTS</b>
SIZE <b>B</b>			DRAWING NUMBER <b>(SC)MKT-SQA48D</b>
FORMERLY: X-01989			REV <b>A</b>
SHEET 1 of 1			