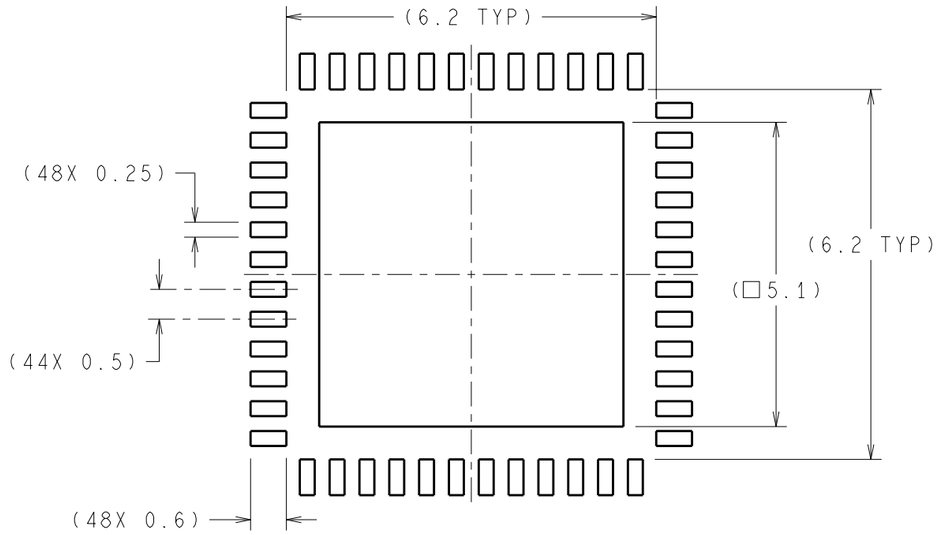
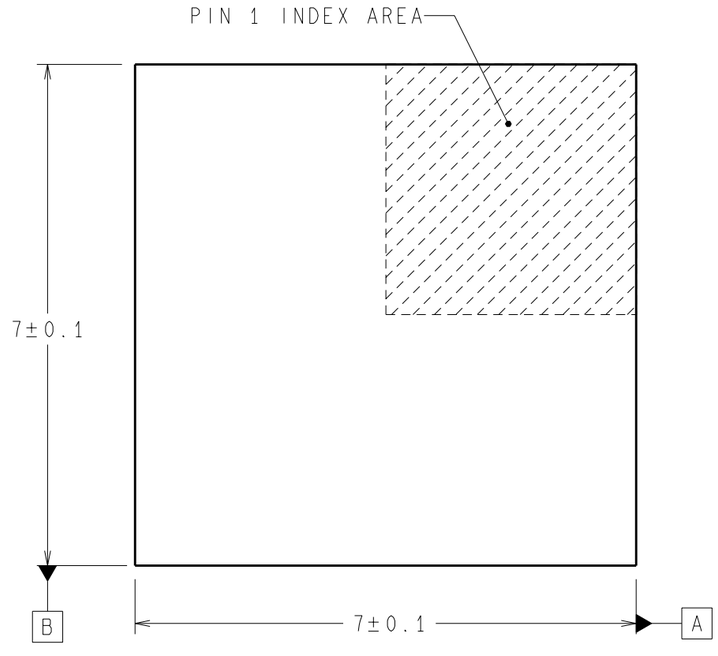
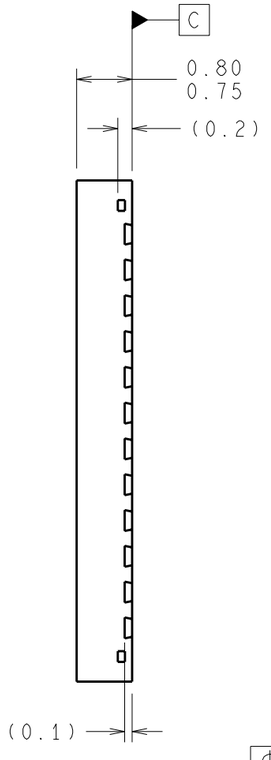
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1012	02/09/2009	LY/TL/EL
B	ADD MINIMUM PACKAGE THICKNESS DIMENSION	2712	05/18/2009	LY/TKY/EL

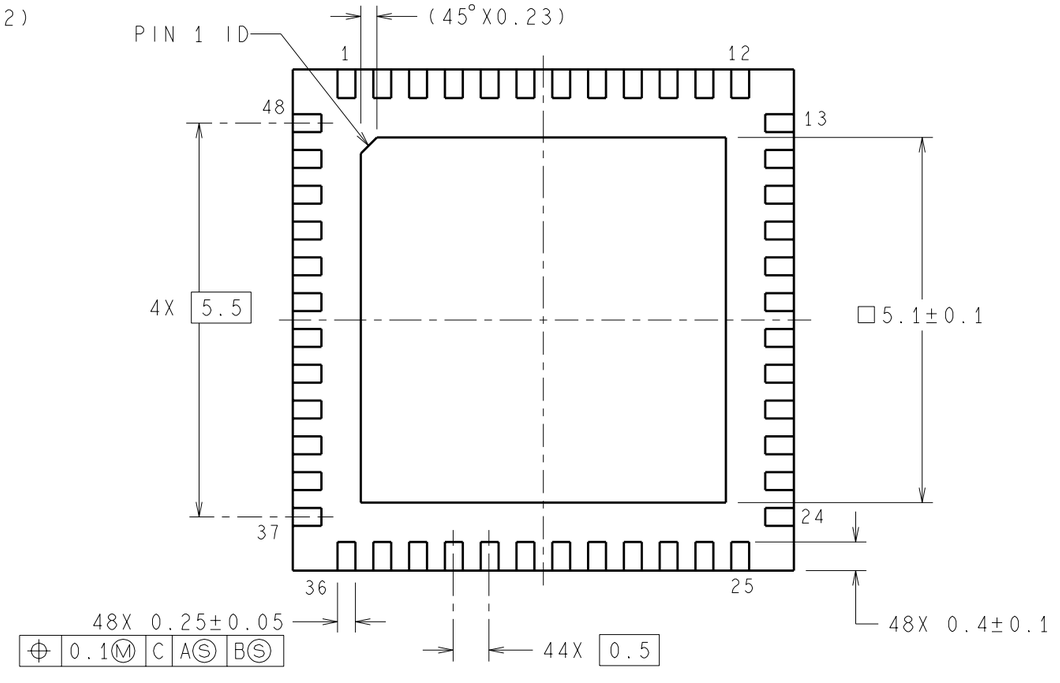


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. REFERENCE JEDEC REGISTRATION MO-220, VARIATION WKKD-2.

APPROVALS	DATE
DRAWN LYE MENG KONG	02/09/2009
DFTG. CHK. TK YII	05/18/2009
ENGR. CHK. EL/CH MAK	05/18/2009

PROJECTION MM

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

LLP, PLASTIC, QUAD,
7x7x0.8mm, 48 LD,
0.5mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SQA48A	B

FORMERLY: N/A | SHEET 1 of 1