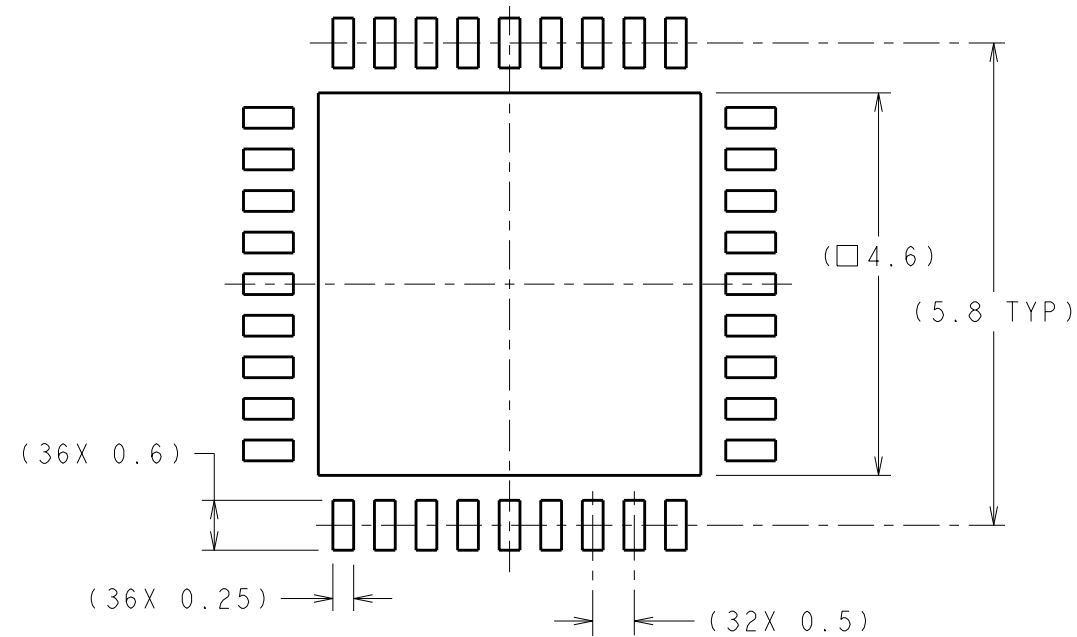
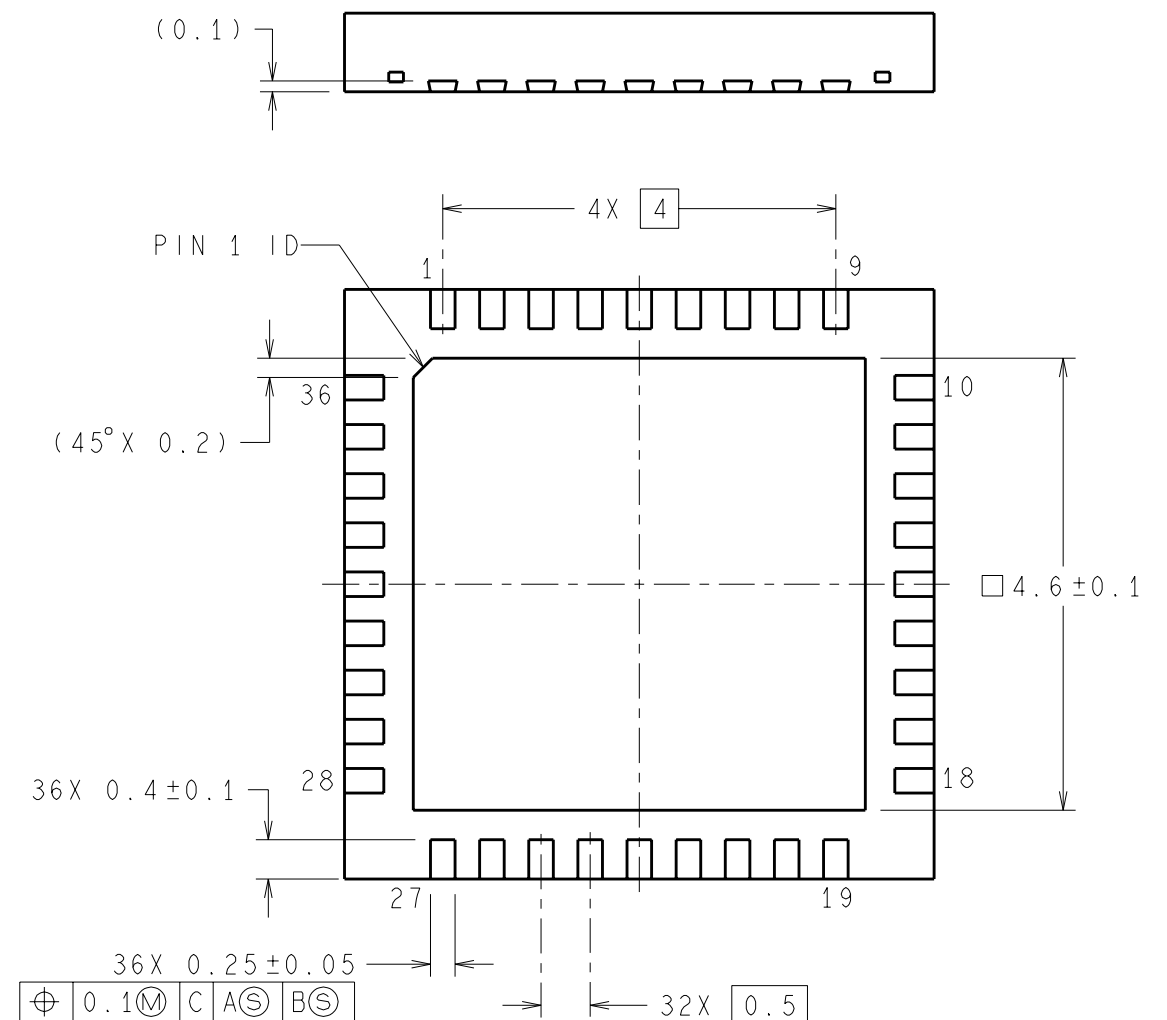
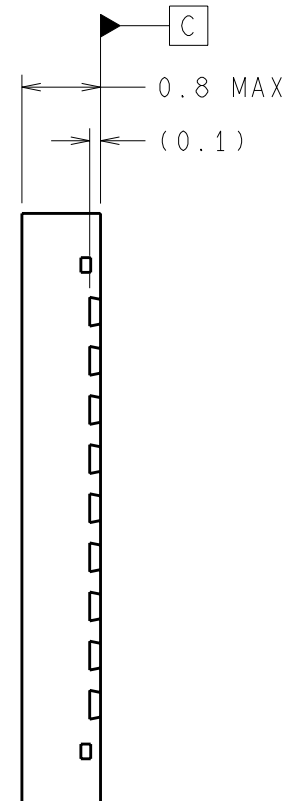
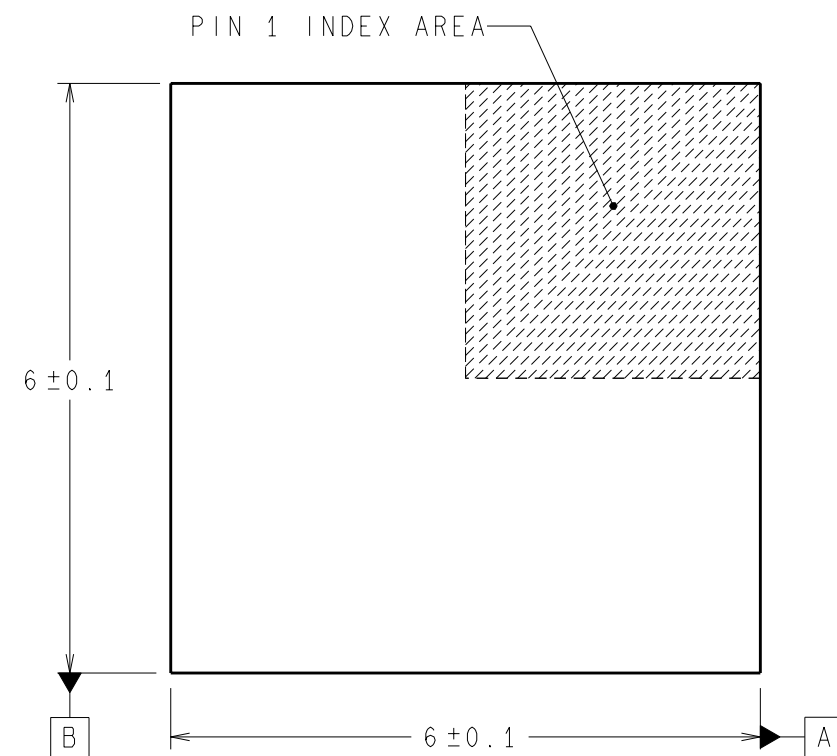


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1085	06/19/2003	HR/TL/SN



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

**RECOMMENDED LAND PATTERN**



NOTES: UNLESS OTHERWISE SPECIFIED.

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE ([www.national.com](http://www.national.com)).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF JUNE 2003.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090			
DRAWN	HAFIZA RAMLEY	06/19/2003				
DFTG. CHK.	THANH LEQUANG	06/19/2003				
ENGR. CHK.	N. SANTHIRAN	06/19/2003				
PROJECTION  MM			SCALE NTS	SIZE B	DRAWING NUMBER (SC)MKT-SQA36A	REV A
FORMERLY: N/A			SHEET 1 of 1			