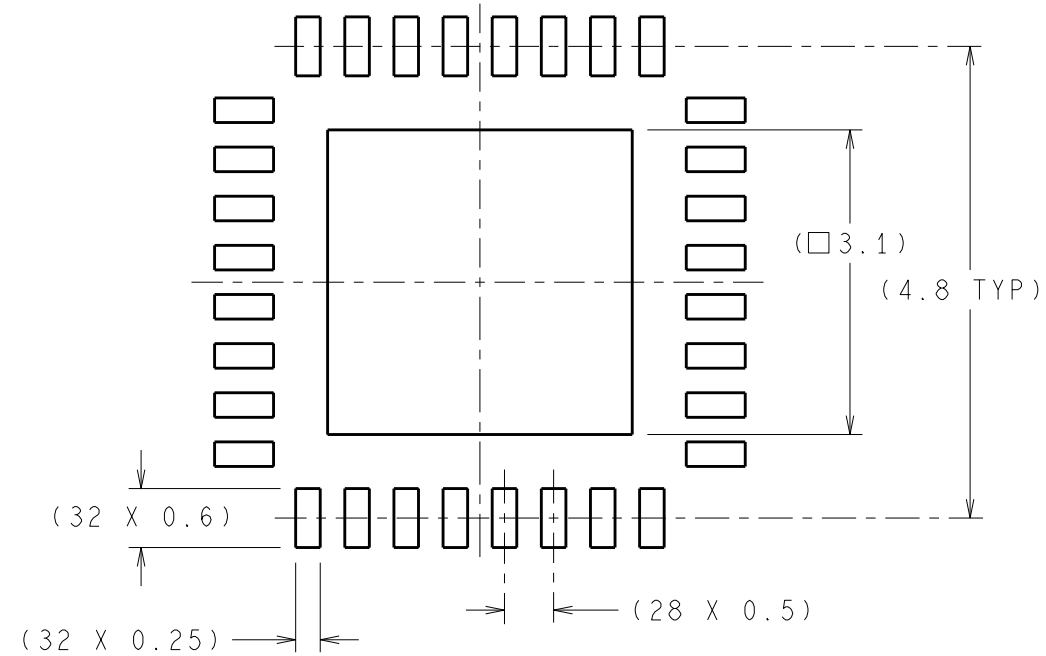
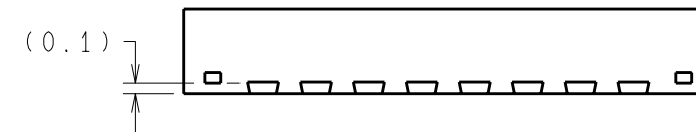


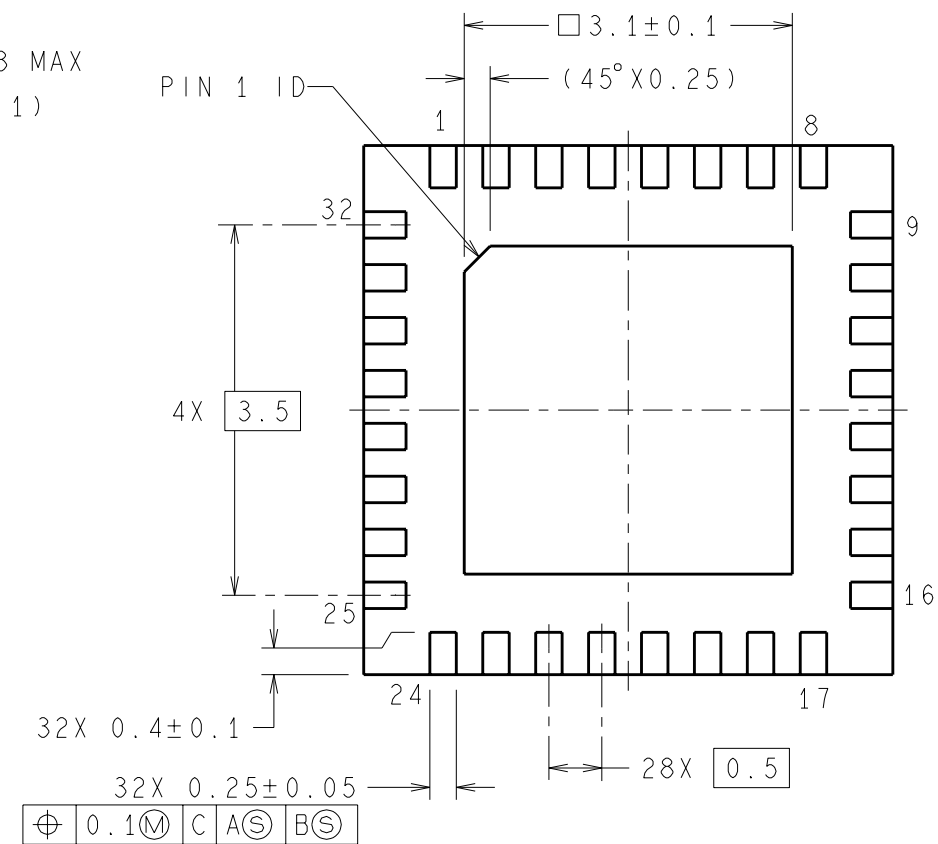
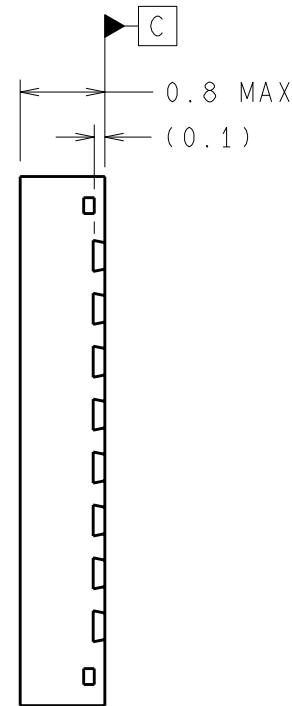
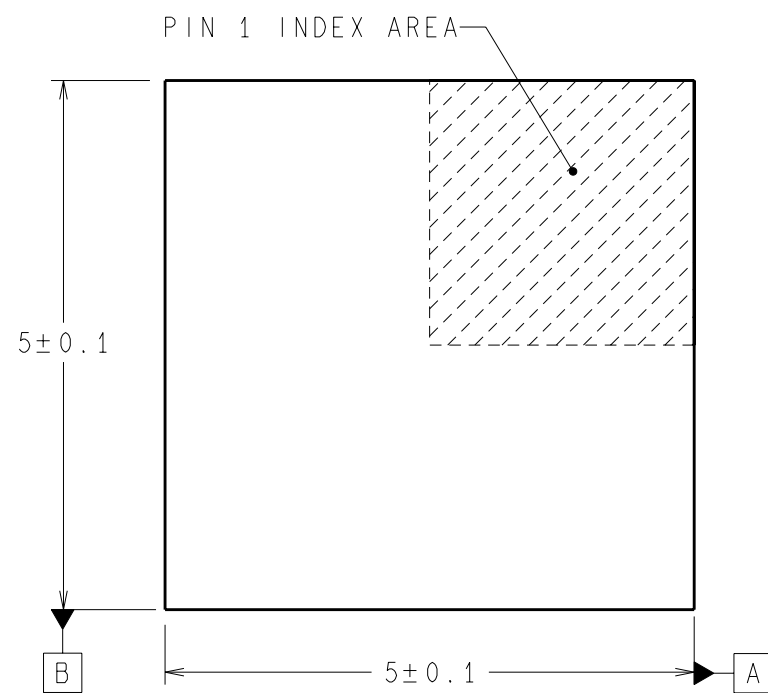
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1456	07/06/2004	HL/MS/SN
B	CHANGE MILLIMETERS TO MILLIMETERS	2918	10/20/2009	SL/EL/LS



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF OCTOBER 2009.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	HENRY LIM	07/06/2004		
DFTG. CHK.	EUGENE LEE	10/20/2009	LLP, QUAD, 5x5x0.8mm, 32 LD, 0.5mm PITCH, NO PULLBACK, 3.1x3.1mm EXP PAD	
ENGR. CHK.	LOREN SIEBERT	10/20/2009		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-SQA32A	B
FORMERLY: N/A			SHEET 1 of 1	