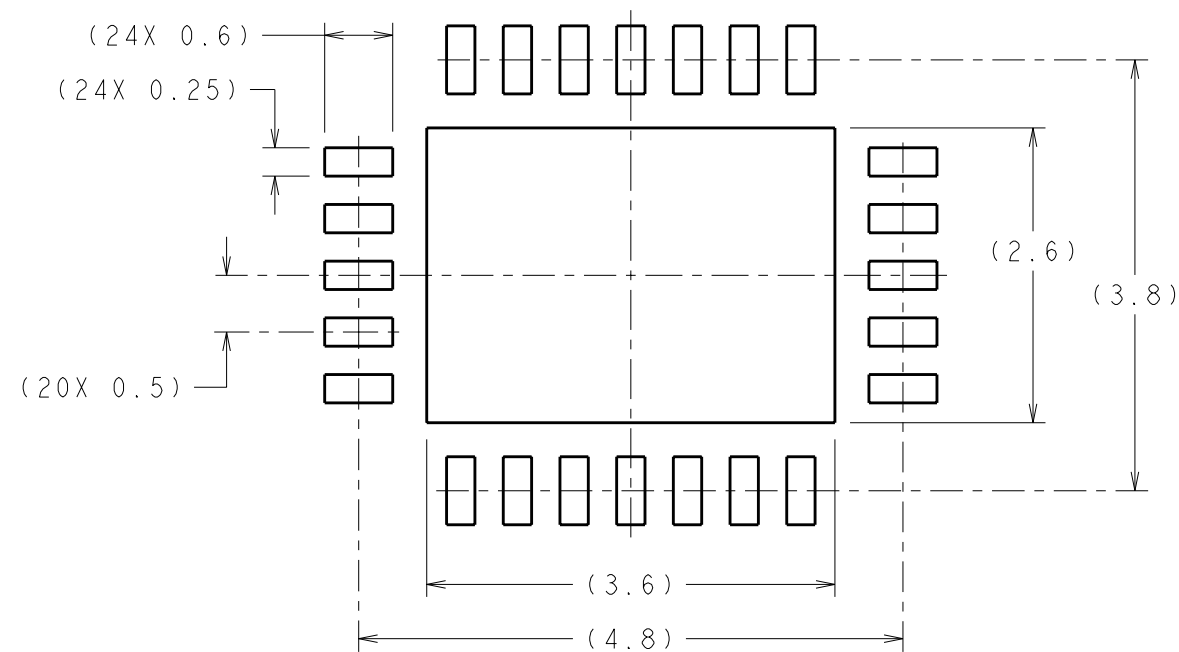
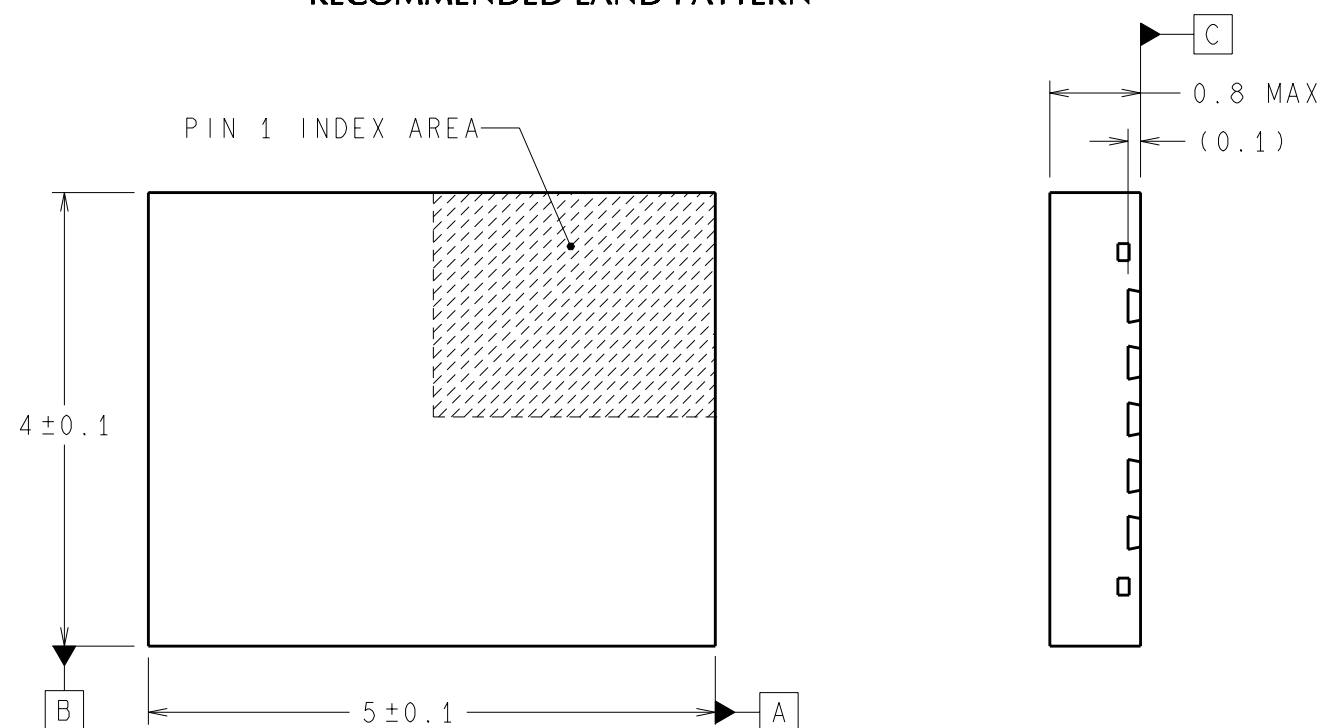


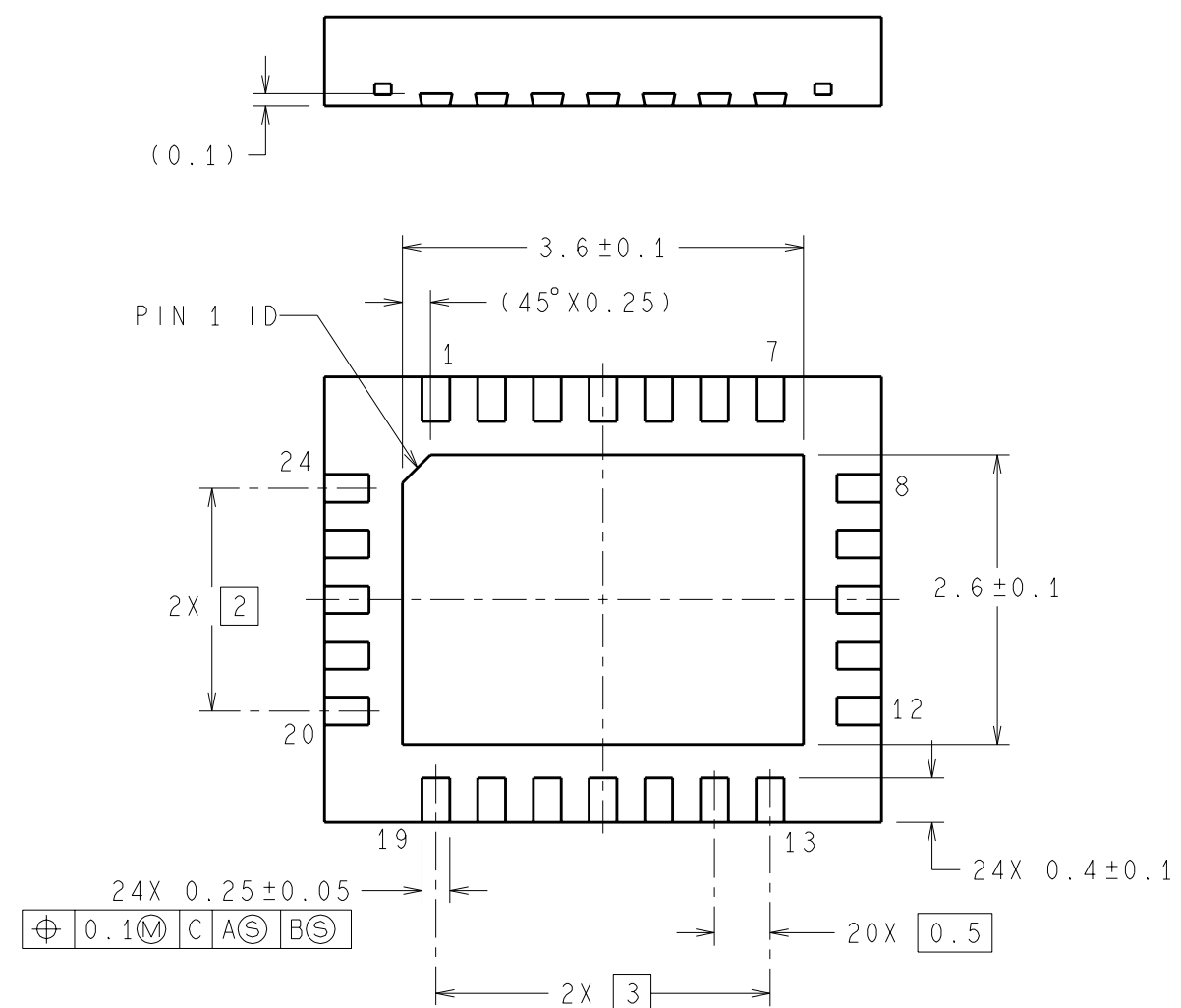
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1179	10/07/2003	AS/TL/SN



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com)
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- REFERENCE JEDEC REGISTRATION MO-220, VARIATION WGHD-1.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN A. SULAIMAN & TL		10/07/2003	
DFTG. CHK. THANH LEQUANG		10/07/2003	
ENGR. CHK. N. SANTHIRAN		10/07/2003	
PROJECTION MM			SCALE NTS
SIZE B			DRAWING NUMBER (SC)MKT-SQA24B
FORMERLY: N/A			REV A

LLP, PLASTIC, QUAD,
5x4x0.8mm BODY, 24 LD,
0.5mm PITCH, NO PULLBACK