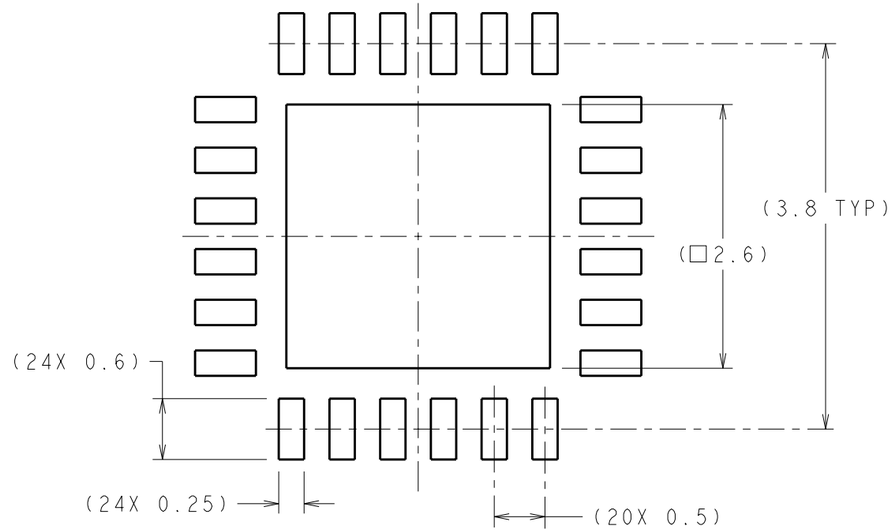
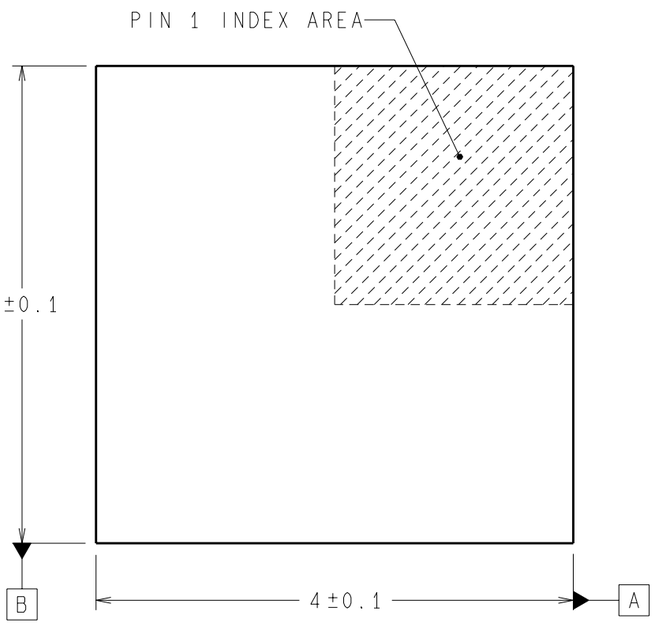
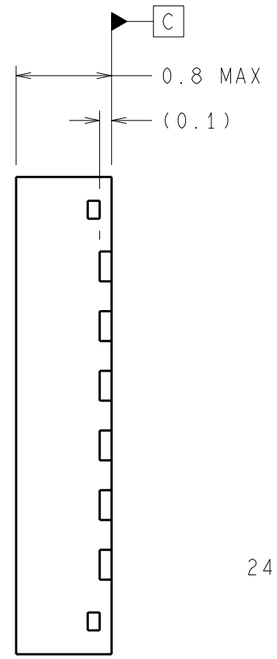
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1007	04/25/2003	TL/AT
B	REVISE TITLE; ADD BURR INFO NOTE, JEDEC INFO & TOP SIDE VIEW; CHANGE LAND PATT DIM PER STD	1050	08/01/2003	TL/AT

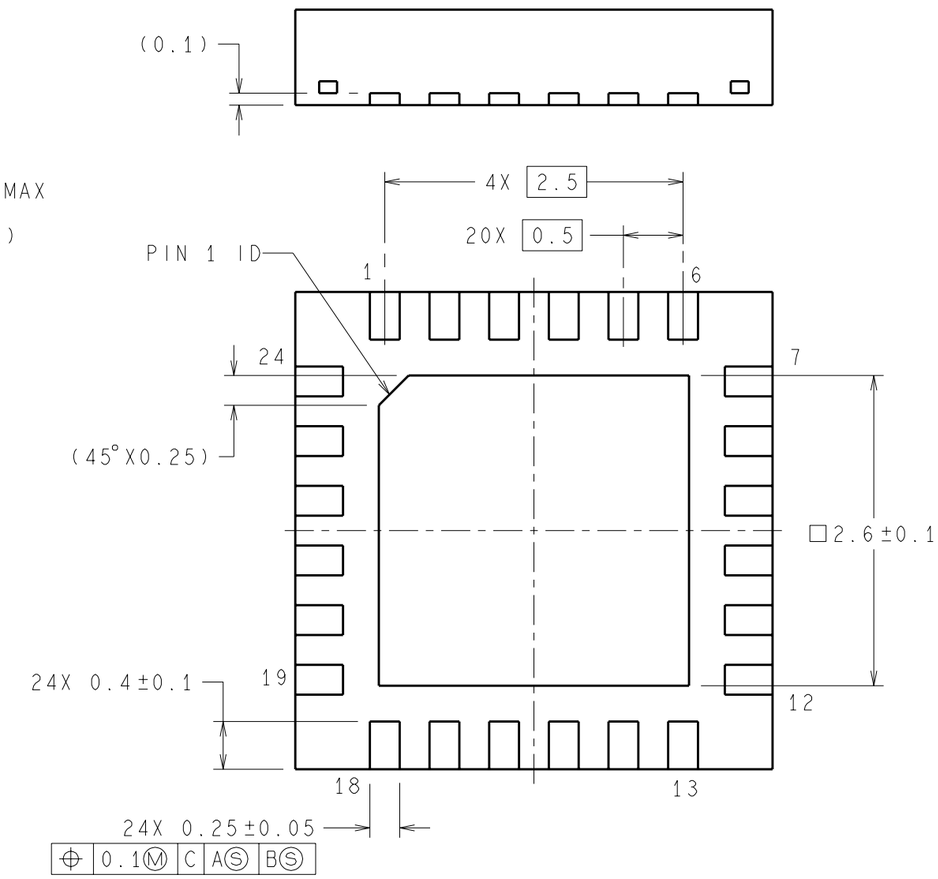


DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN







NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. REFERENCE JEDEC REGISTRATION MO-220, WGGD-6.

APPROVALS	DATE
DRAWN T. LEQUANG	04/17/2003
DFTG. CHK. MARTA SUCHY	08/01/2003
ENGR. CHK. ANNY TU	08/01/2003

PROJECTION MM

National Semiconductor
2900 Semiconductor Dr, Santa Clara, CA 95052-8090

LLP, PLASTIC, QUAD, 4x4x0.8mm BODY, 24 LD, 0.5mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SQA24A	B

FORMERLY: X-01939 SHEET 1 of 1