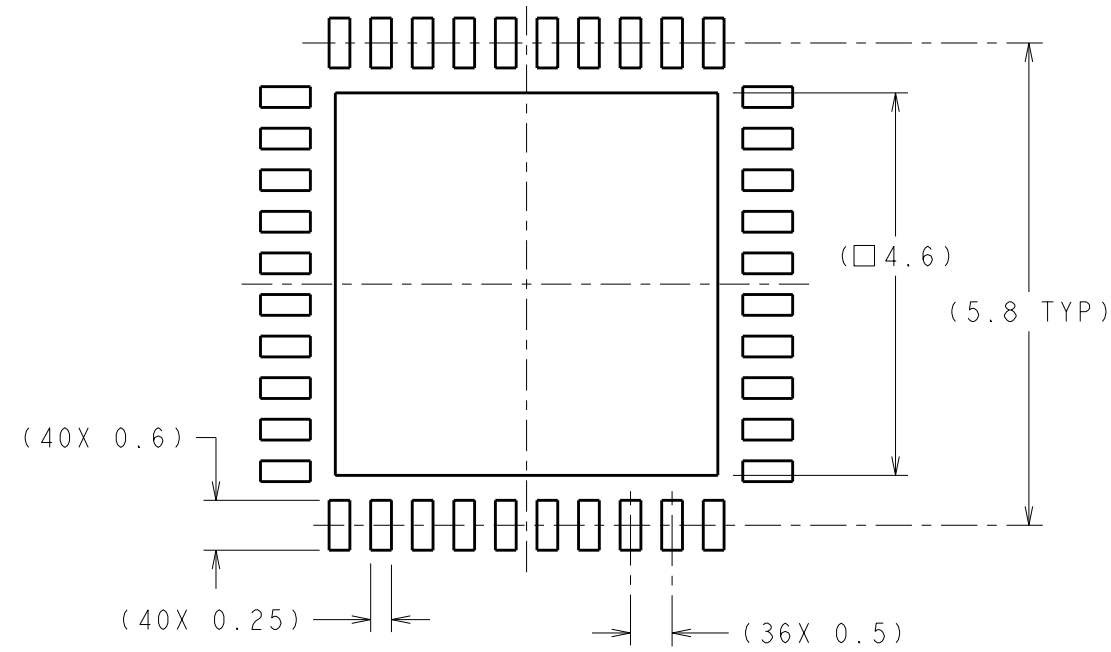
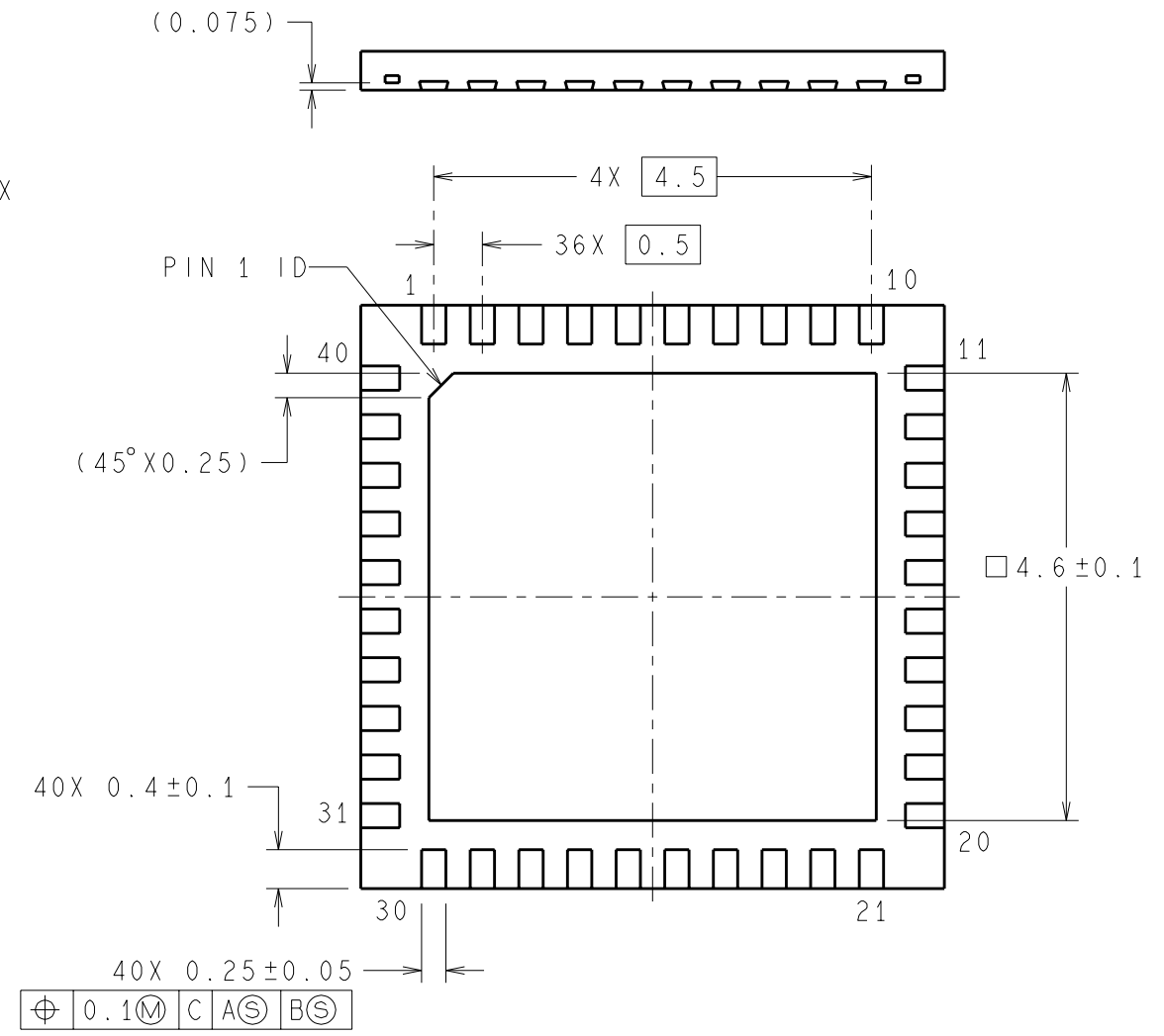
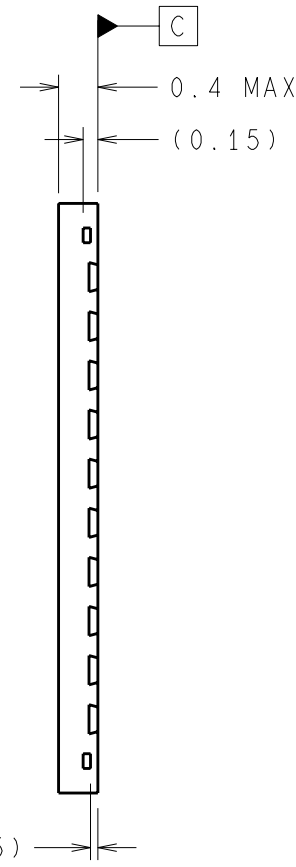
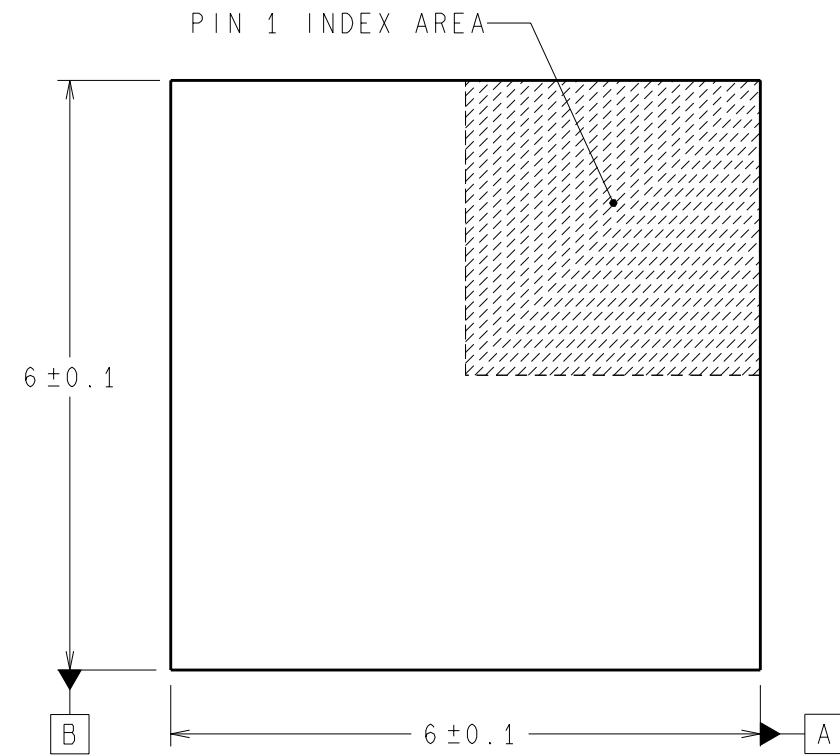


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1755	03/16/2005	AS/TL/SN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



⊕	0.1	Ⓜ	C	A	Ⓢ	B	Ⓢ
---	-----	---	---	---	---	---	---

NOTES: UNLESS OTHERWISE SPECIFIED.

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF MARCH 2005.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	A. SULAIMAN & TL	03/16/2005		
DFTG. CHK.	THANH LEQUANG	03/16/2005	THIN LLP, QUAD, 6x6x0.4mm, 40 LD, 0.5mm PITCH, NO PULLBACK	
ENGR. CHK.	N. SANTHIRAN	03/16/2005		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-SNA40A	A
FORMERLY: N/A			SHEET 1 of 1	