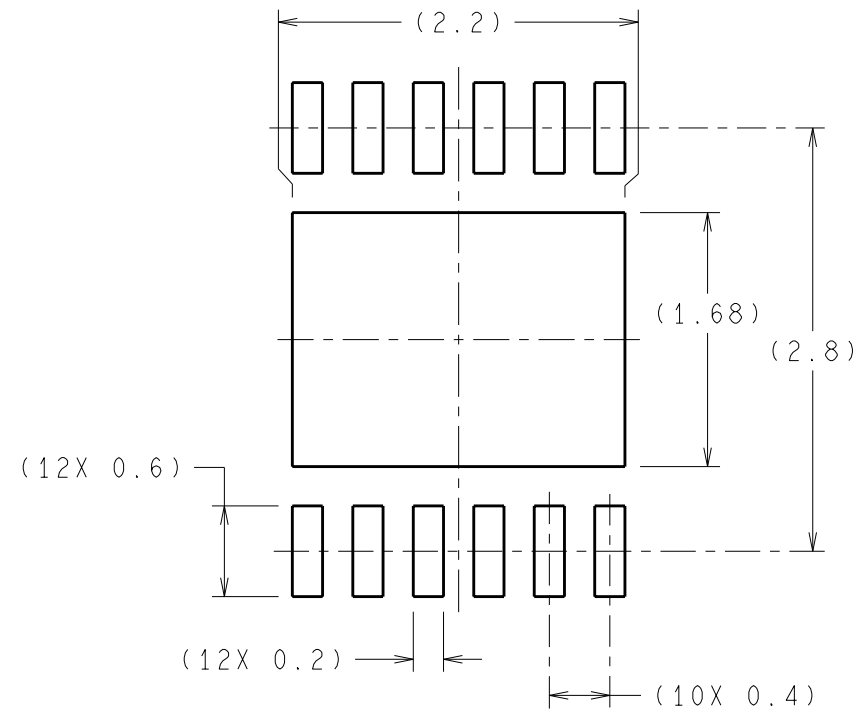
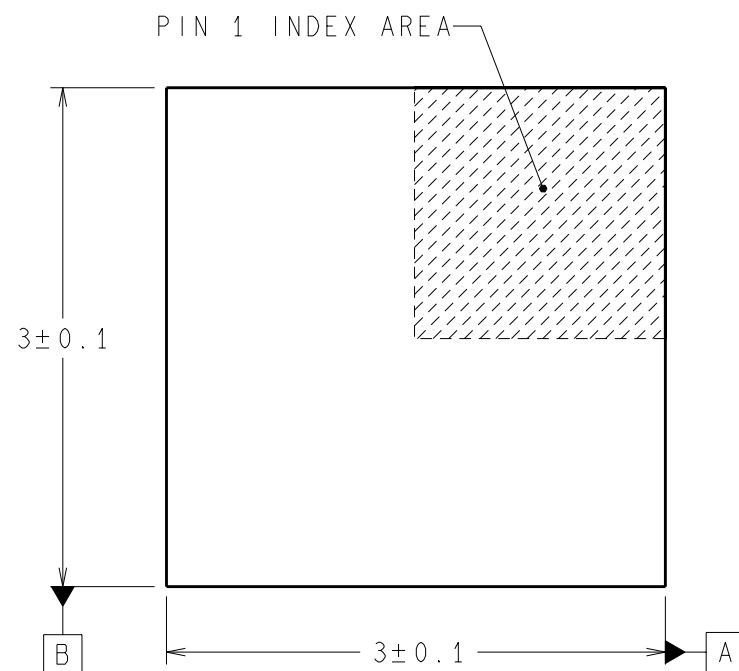


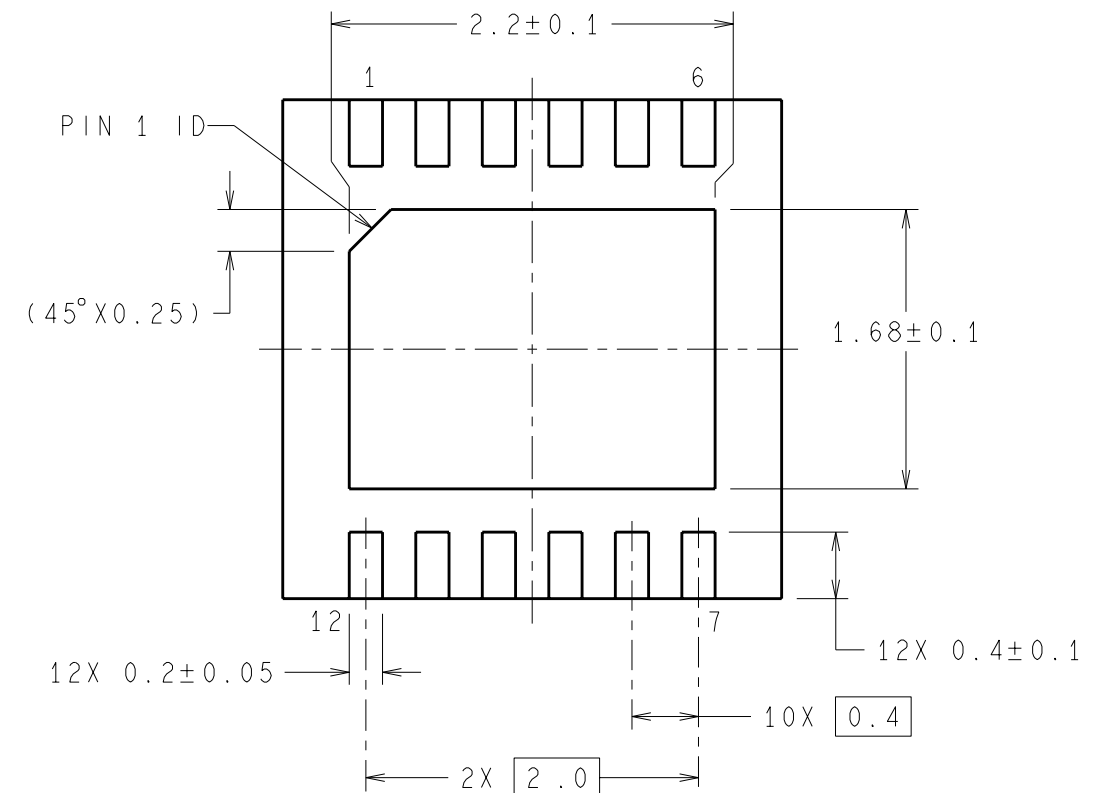
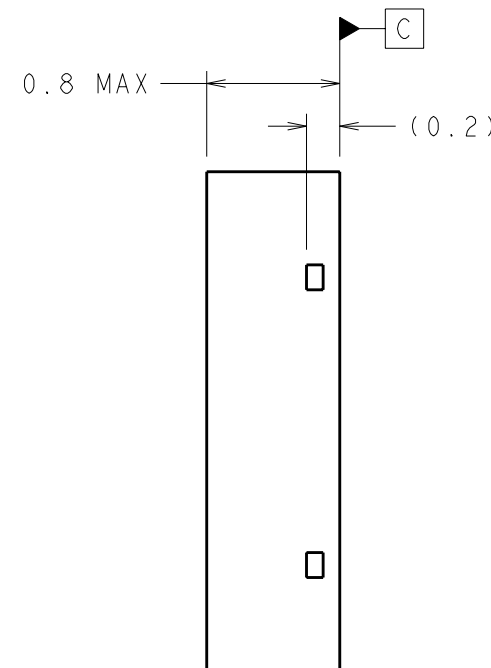
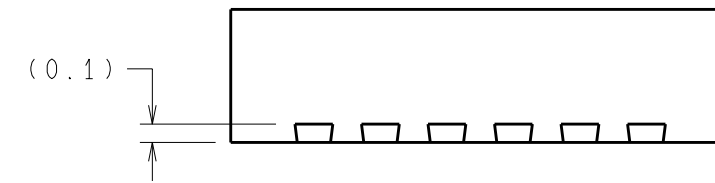
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1929	10/03/2005	AS/MS/SN
B	CORRECT THE LEAD NUMBER ON PACKAGE BOTTOM VIEW	2469	07/08/2008	EL/TL/EL



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF JULY 2008.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090		
DRAWN	A. SULAIMAN	10/03/2005			
DFTG. CHK.	THANH LEQUANG	07/08/2008	LLP, PLASTIC, DUAL, 3x3x0.8mm, 12 LD, 0.4mm PITCH, NO PULLBACK		
ENGR. CHK.	EUGENE LEE	07/08/2008			
PROJECTION	MM	SCALE	SIZE	DRAWING NUMBER	REV
		NTS	B	(SC)MKT-SDF12A	B
FORMERLY: N/A				SHEET 1 of 1	