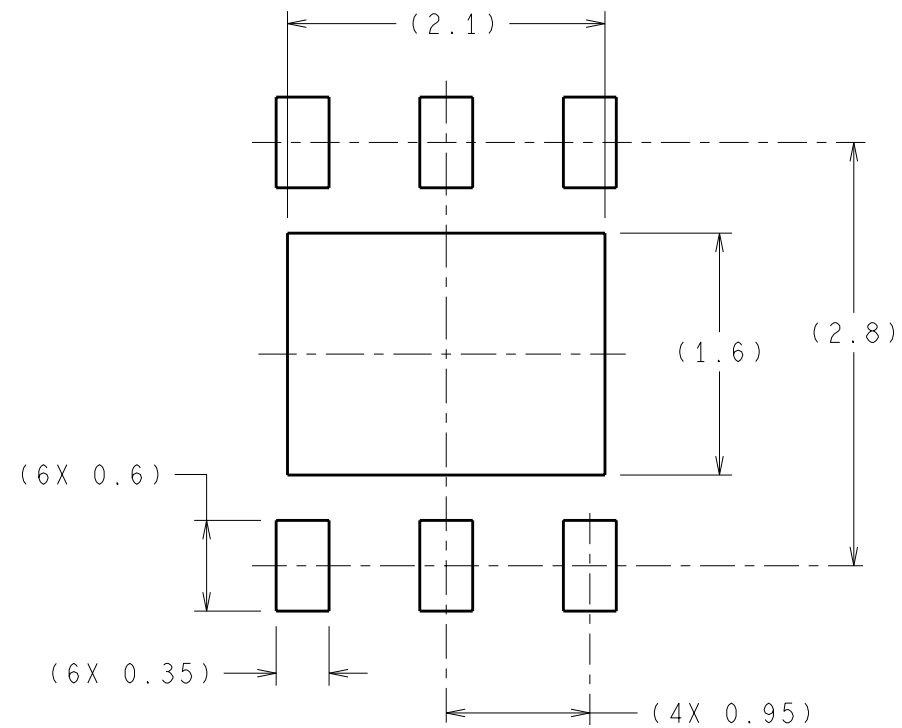
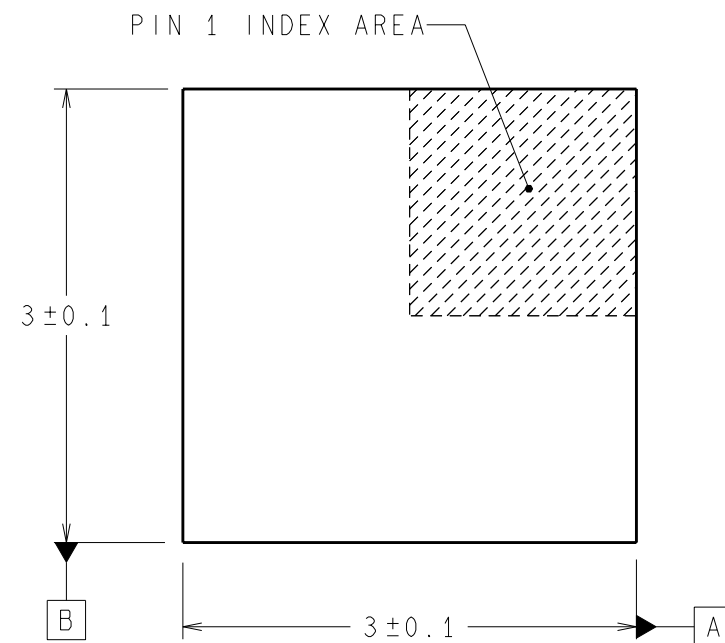


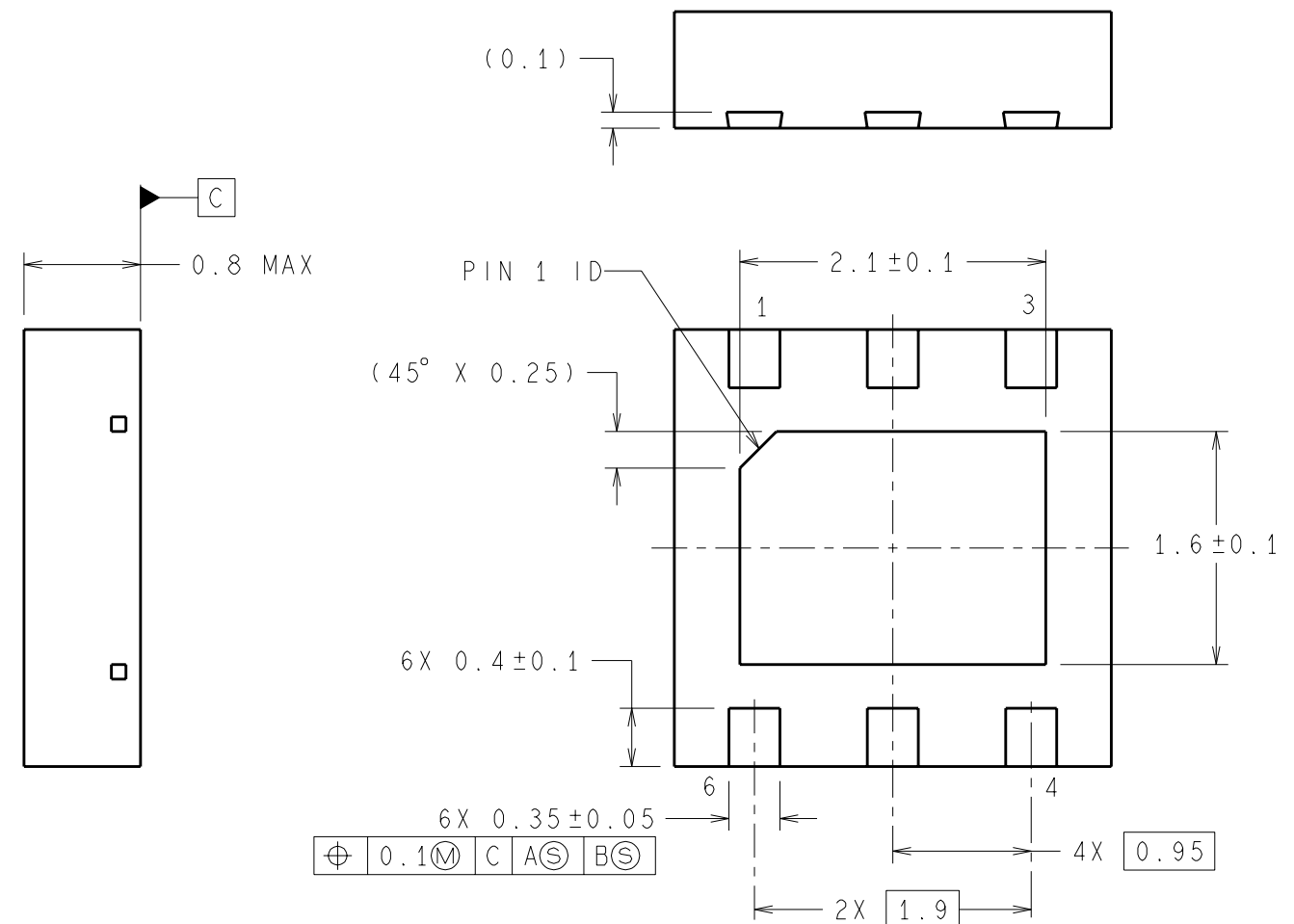
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1088	07/01/2003	AS/TL/SN



**RECOMMENDED LAND PATTERN**



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSION IN ( ) FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE ([www.national.com](http://www.national.com)).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRON.
3. NO JEDEC REGISTRATION AS OF JULY 2003.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	ASNOR SULAIMAN	07/01/2003		
DFTG. CHK.	THANH LEQUANG	07/01/2003	<b>LLP, PLASTIC, DUAL,</b> <b>3x3x0.8mm BODY, 6 LD,</b> <b>0.95mm PITCH, NO PULLBACK</b>	
ENGR. CHK.	SANTHIRAN N	07/01/2003		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-SDE06A	A
FORMERLY: N/A			SHEET 1 of 1	