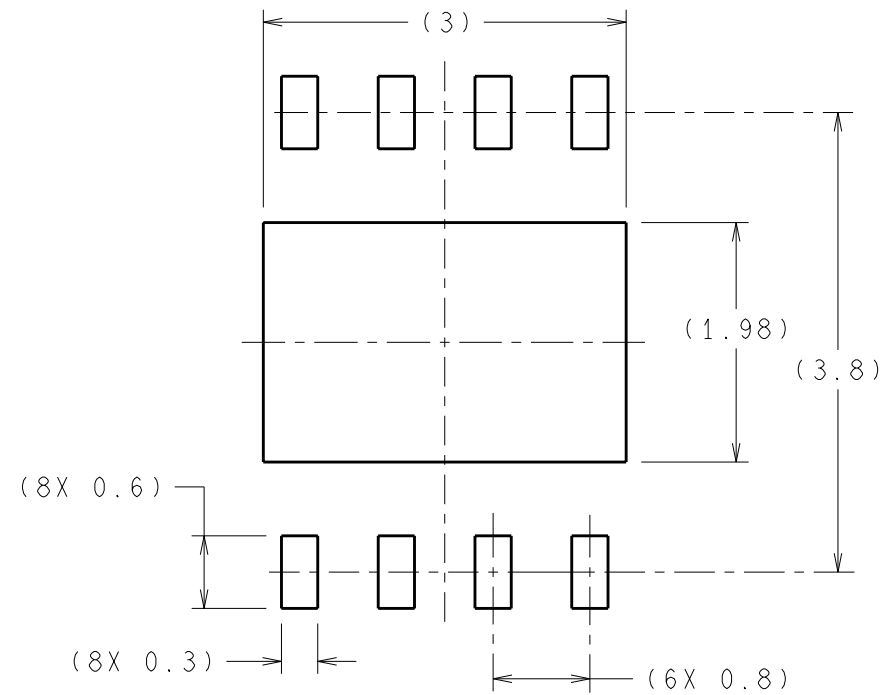
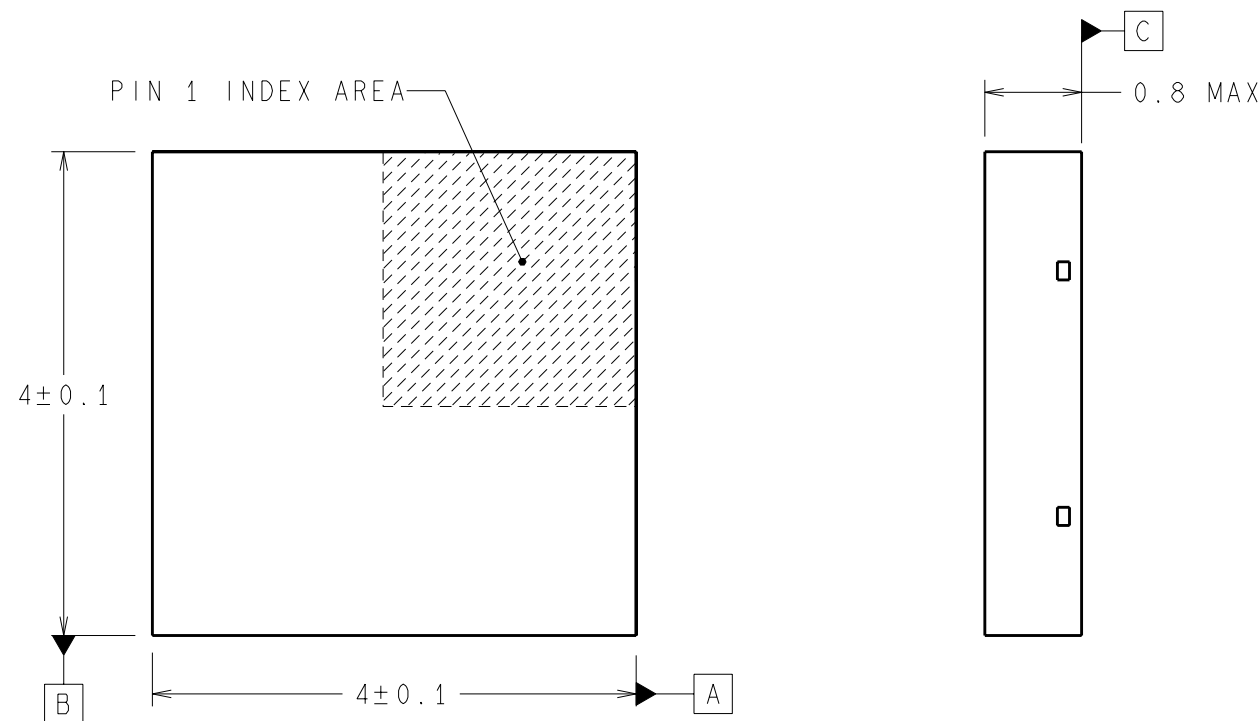


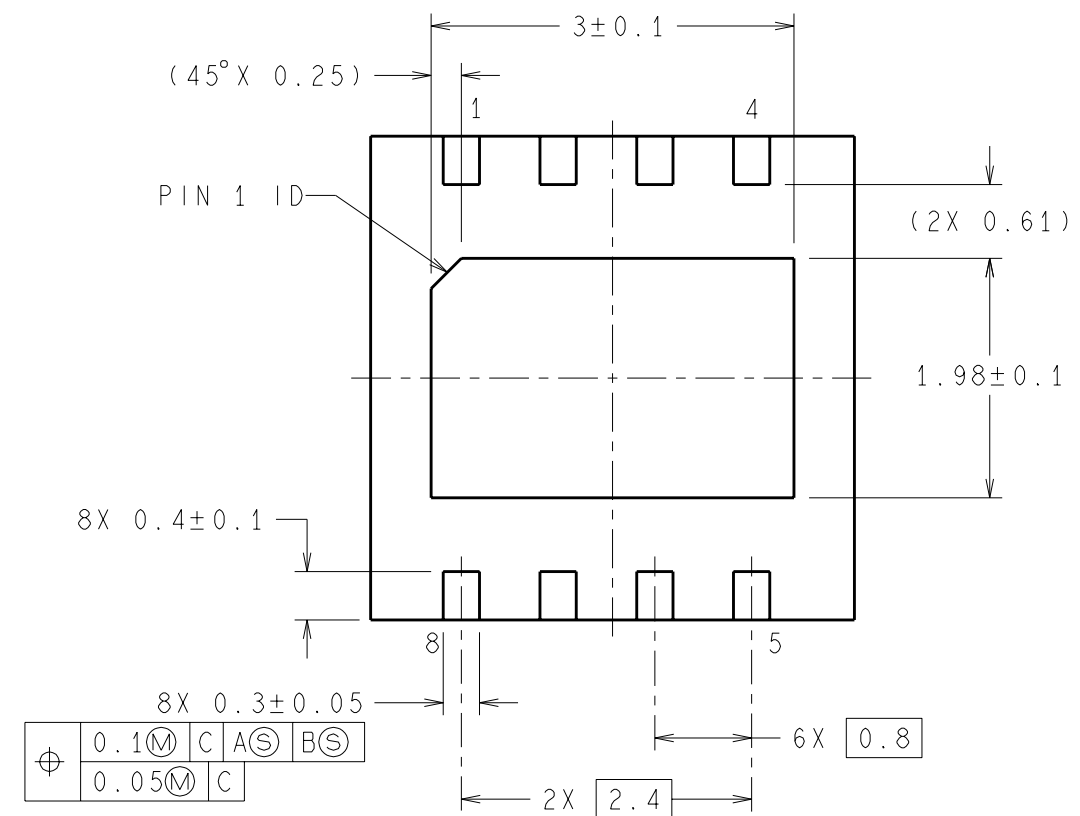
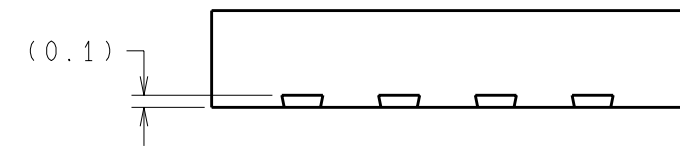
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2056	03/28/2006	AS/TL/AS



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



⊕	0.1(M)	C	A(S)	B(S)
	0.05(M)	C		

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF MARCH 2006.

APPROVALS		DATE	National Semiconductor	
DRAWN	ASNOR SULAIMAN	03/28/2006	2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DFTG. CHK.	THANH LEQUANG	03/28/2006	LLP, DUAL, 4x4x0.8mm, 8 LD, 0.8mm PITCH, NO PULLBACK, 1.98x3mm EXP DAP	
ENGR. CHK.	ASNOR SULAIMAN	03/28/2006		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
MM	NTS	B	(SC)MKT-SDC08B	A
FORMERLY: N/A			SHEET 1 of 1	