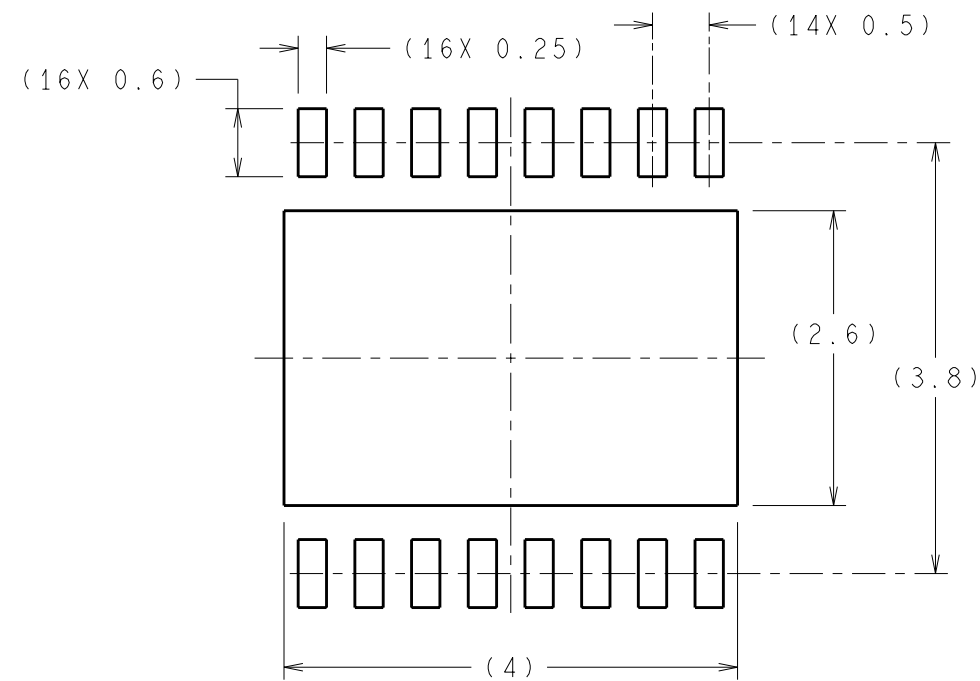
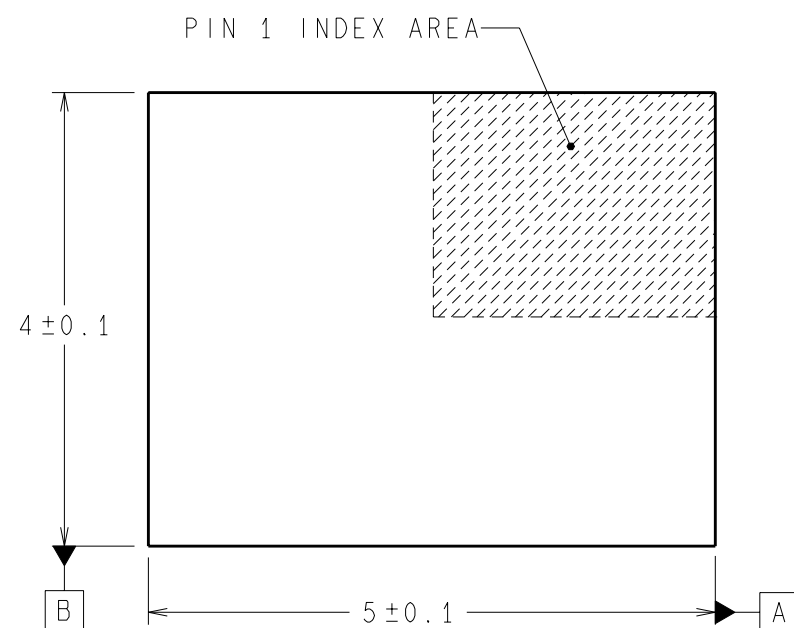


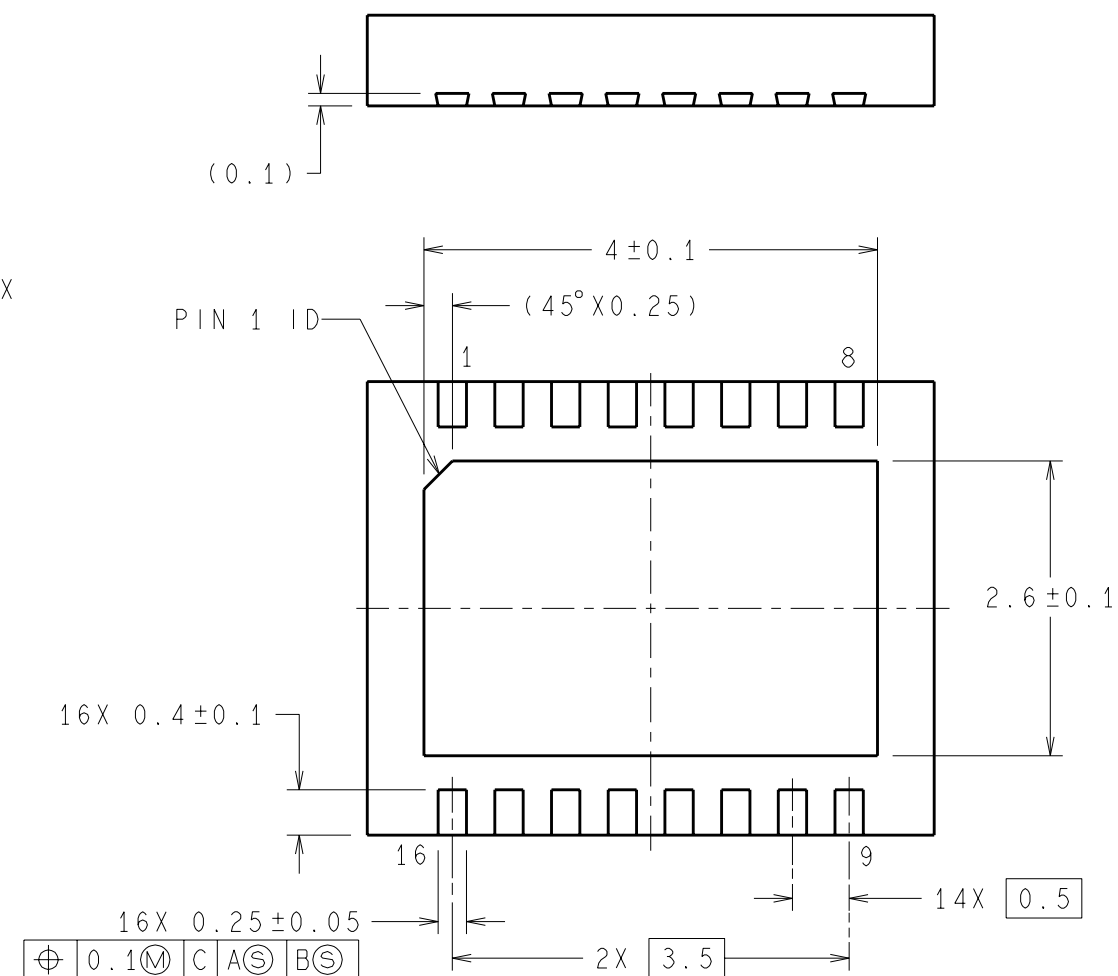
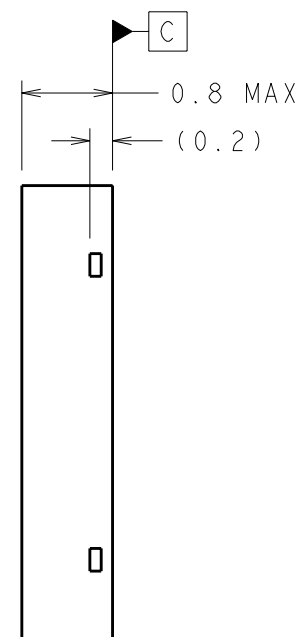
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1706	12/17/2004	AS/MS/SN



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com)
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF DECEMBER 2004.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	ASNOR SULAIMAN	12/17/2004		
DFTG. CHK.	MARTA SUCHY	12/17/2004	LLP, PLASTIC, DUAL, 5x4x0.8mm, 16 LD, 0.5mm PITCH, NO PULLBACK	
ENGR. CHK.	N. SANTHIRAN	12/17/2004		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-SDA16B	A
FORMERLY: N/A			SHEET 1 of 1	