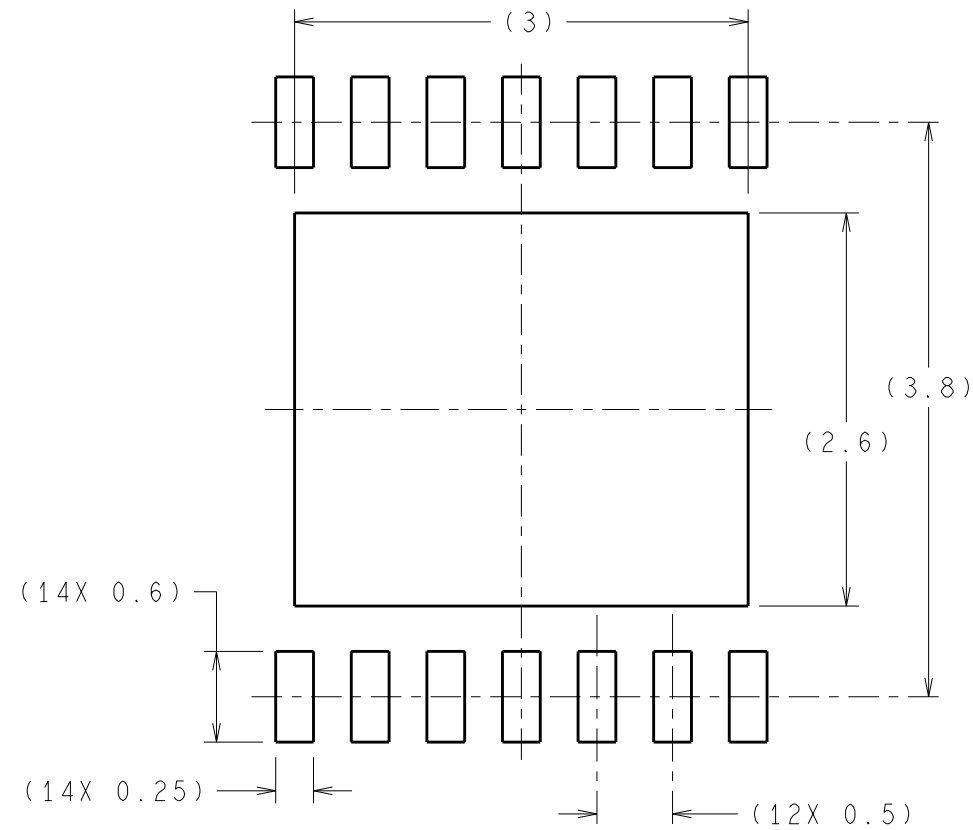
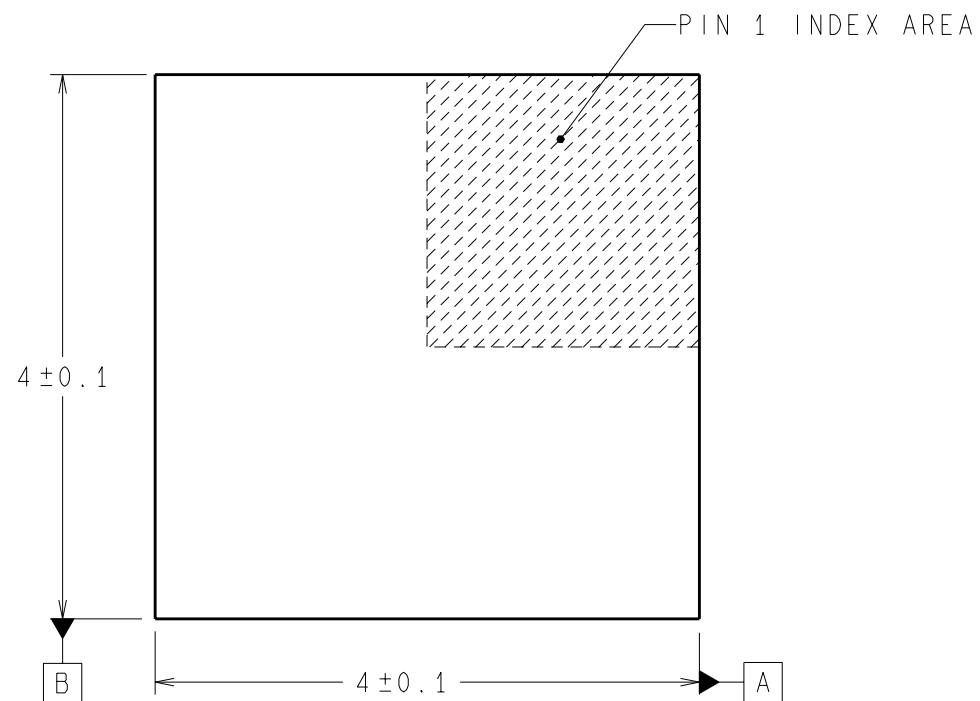


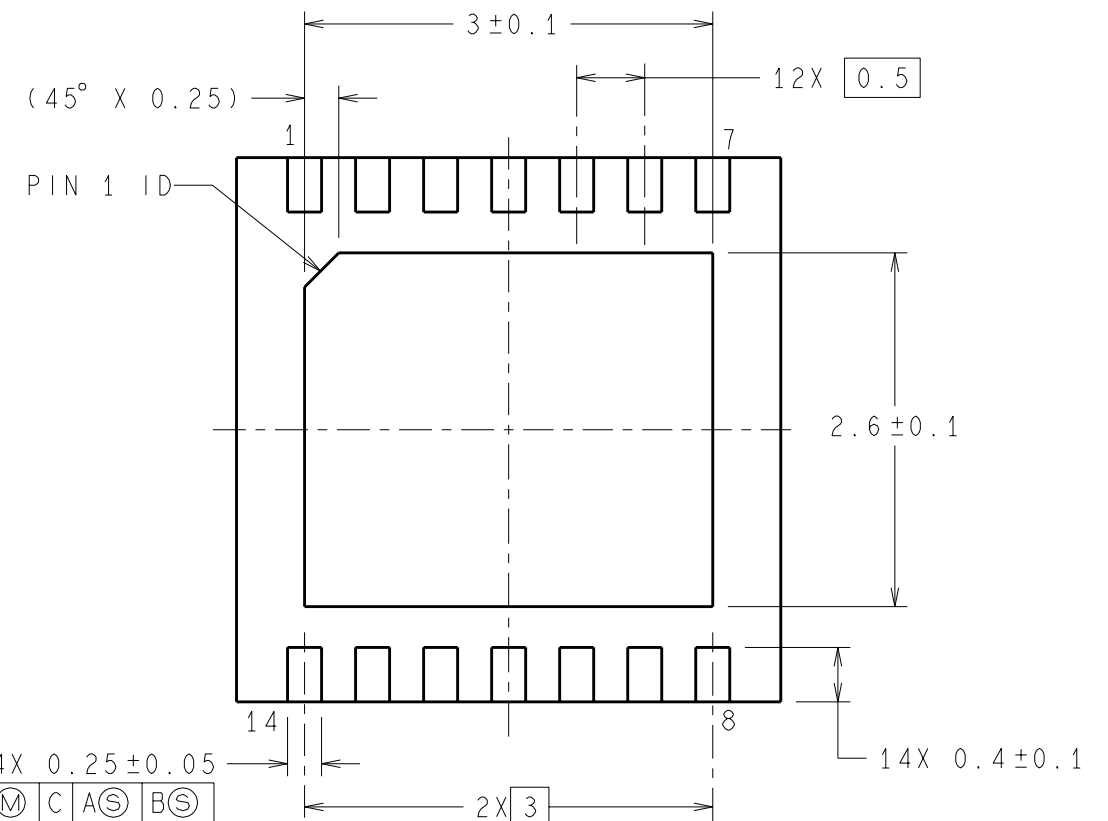
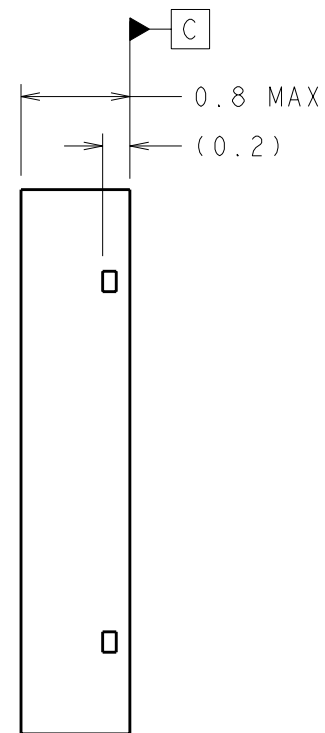
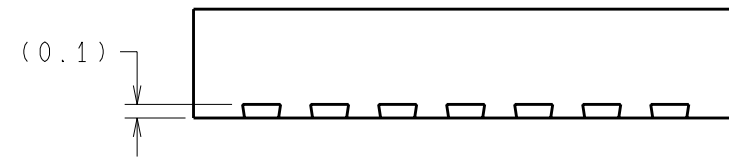
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1553	07/07/2004	AS/MS/SN



**RECOMMENDED LAND PATTERN**



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED.

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE ([www.national.com](http://www.national.com))
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF JUNE 2004.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN <b>ASNOR SULAIMAN</b>		07/07/2004	
DFTG. CHK. <b>MARTA SUCHY</b>		07/07/2004	
ENGR. CHK. <b>N. SANTHIRAN</b>		07/07/2004	
PROJECTION  MM			<b>LLP, DUAL,</b> <b>4x4x0.8mm, 14 LD,</b> <b>0.5mm PITCH, NO PULLBACK</b>
SCALE <b>NTS</b>	SIZE <b>B</b>	DRAWING NUMBER <b>(SC)MKT-SDA14B</b>	REV <b>A</b>
FORMERLY: N/A		SHEET 1 of 1	