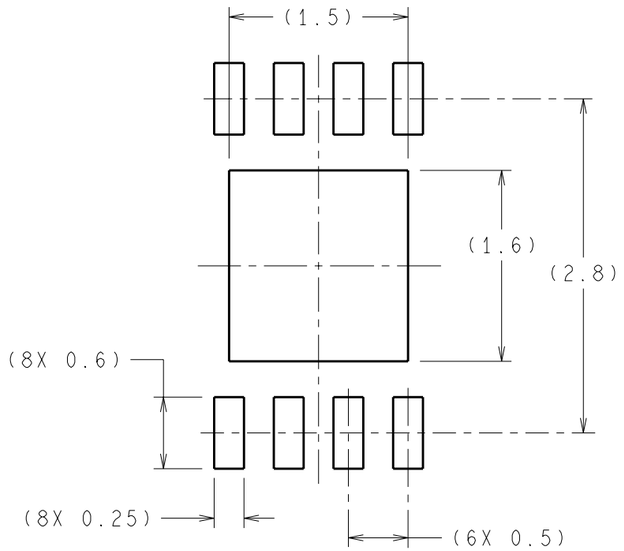
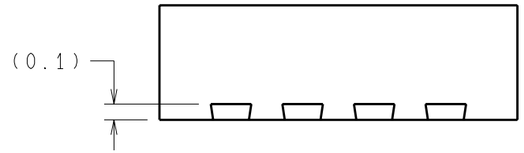
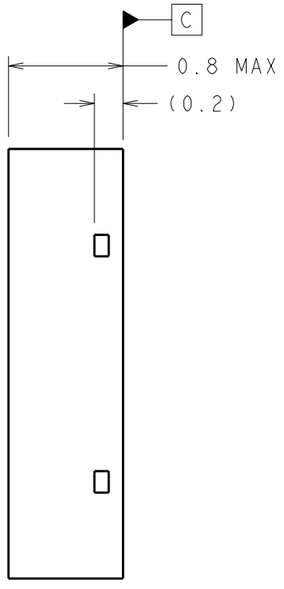
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1267	01/27/2004	AS/TL/SN

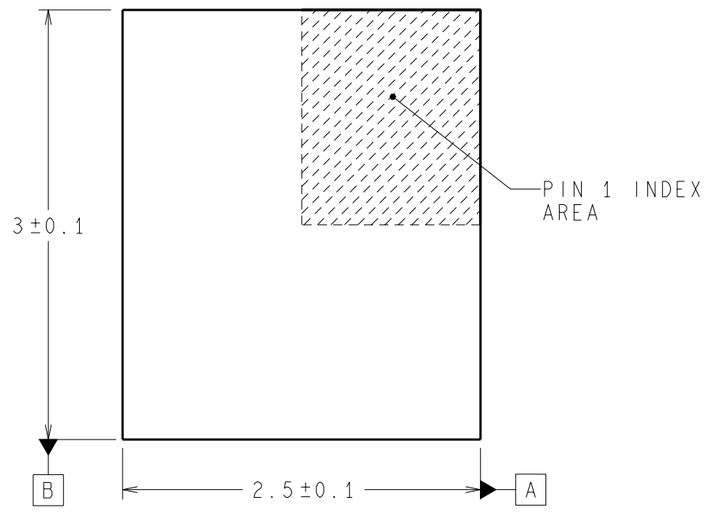


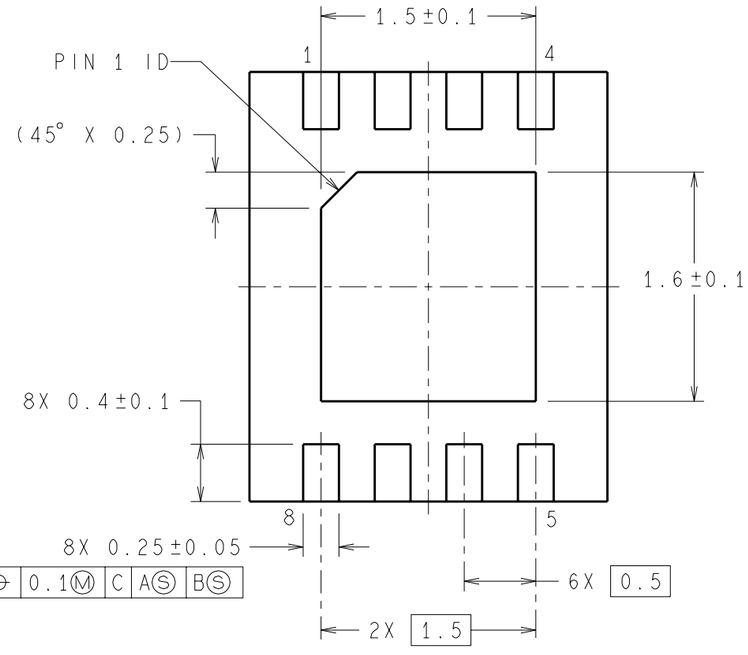
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF JANUARY 2004.

APPROVALS	DATE
DRAWN: ASNOR SULAIMAN	01/27/2004
DFTG. CHK.: THANH LEQUANG	01/27/2004
ENGR. CHK.: N. SANTHIRAN	01/27/2004

PROJECTION MM

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

LLP, PLASTIC, DUAL, 2.5X3X 0.8 mm BODY, 8 LD, 0.5 mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SDA08C	A

FORMERLY: N/A | SHEET 1 of 1