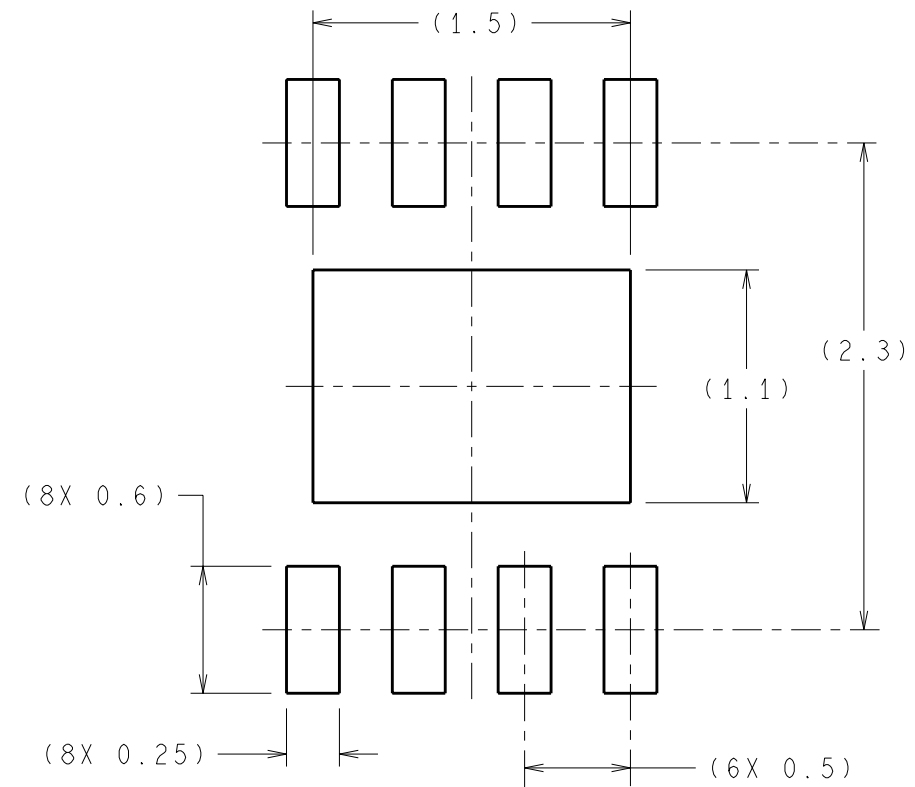
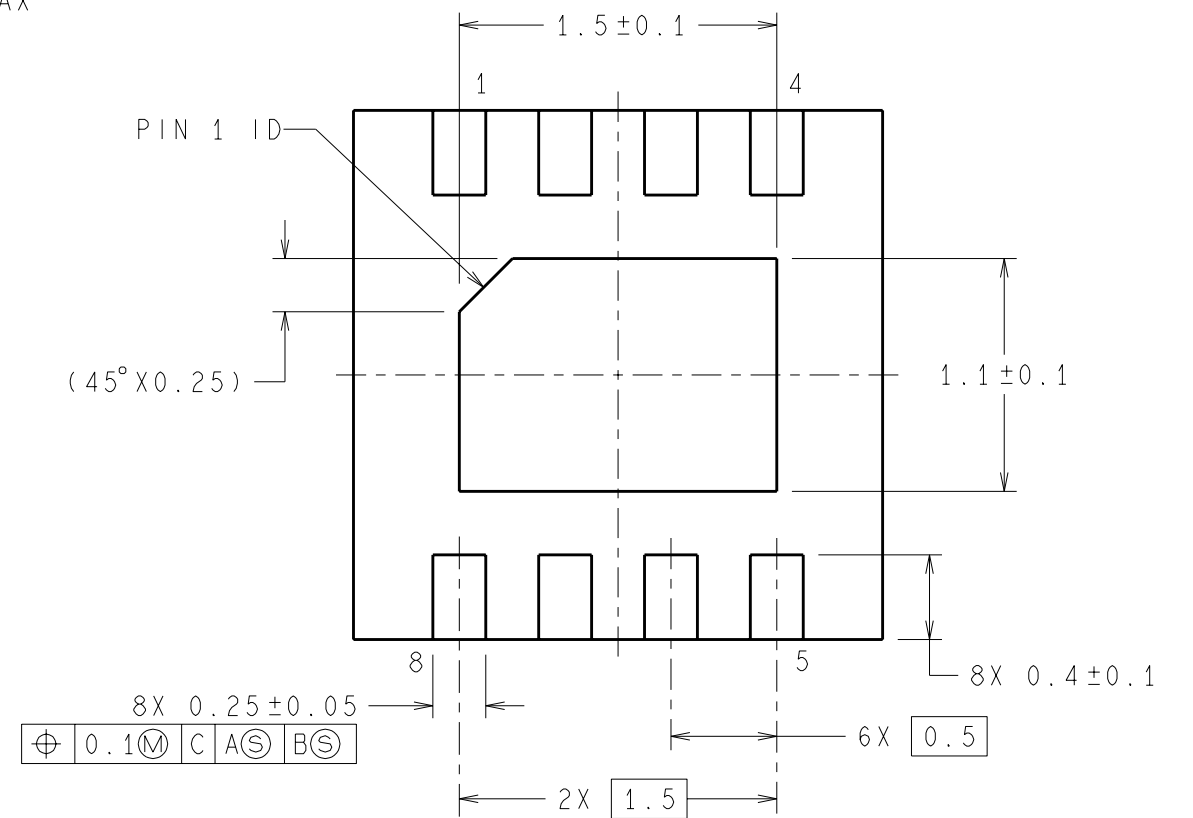
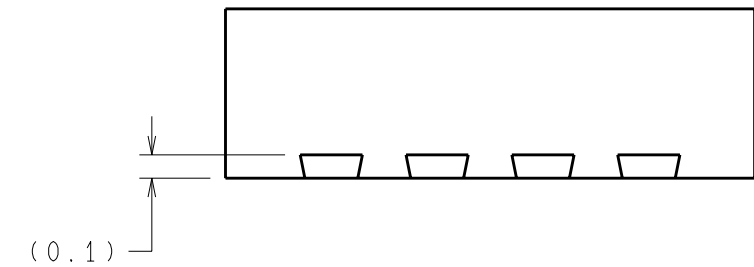
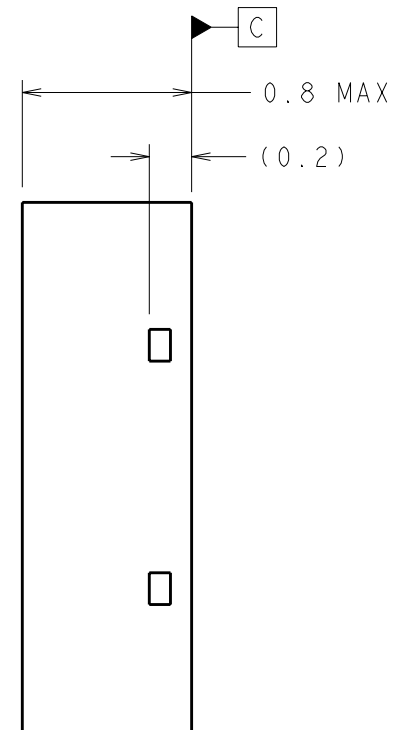
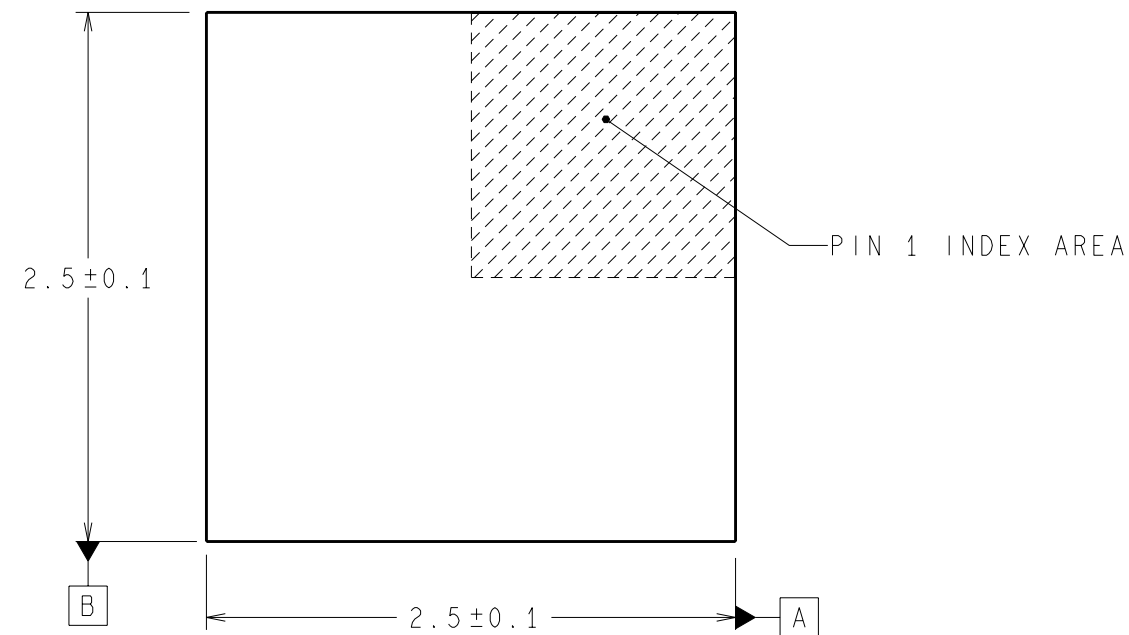


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1266	11/05/2003	AS/MS/SN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF NOVEMBER 2003.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN	ASNOR SULAIMAN	11/05/2003	
DFTG. CHK.	MARTA SUCHY	11/05/2003	
ENGR. CHK.	N. SANTHIRAN	11/05/2003	
PROJECTION:			SCALE: NTS SIZE: B DRAWING NUMBER: (SC)MKT-SDA08B REV: A
FORMERLY: N/A			SHEET 1 of 1