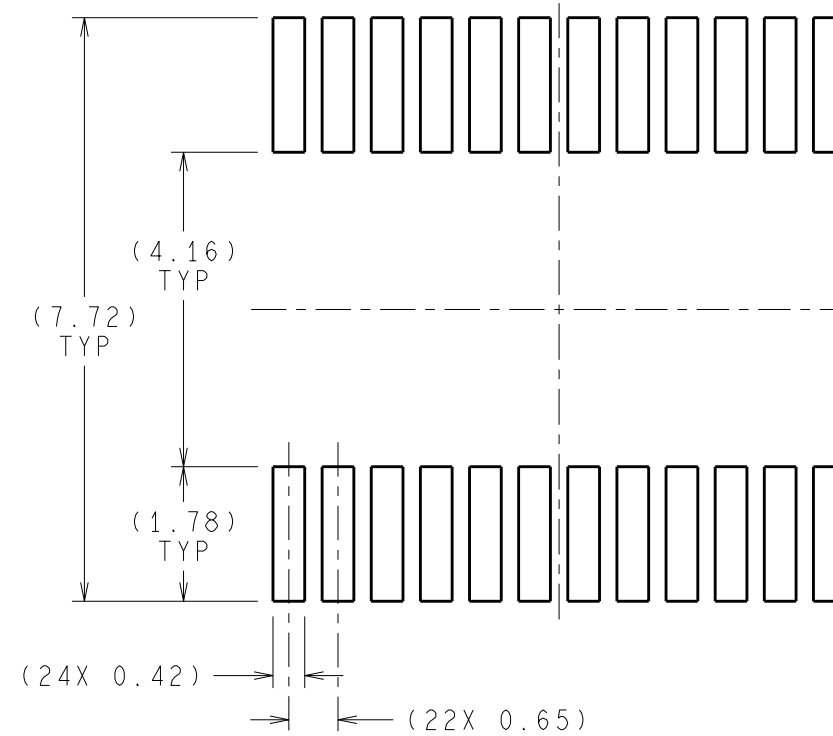
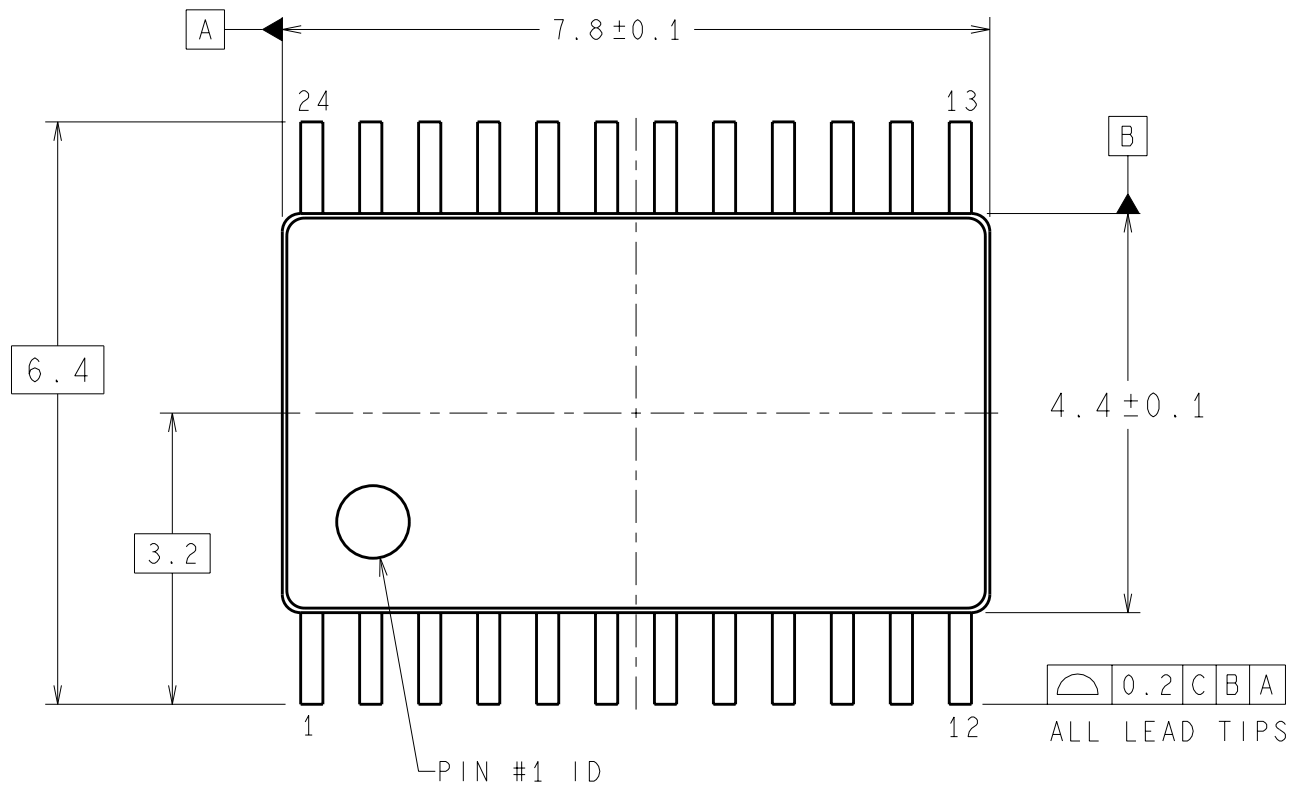
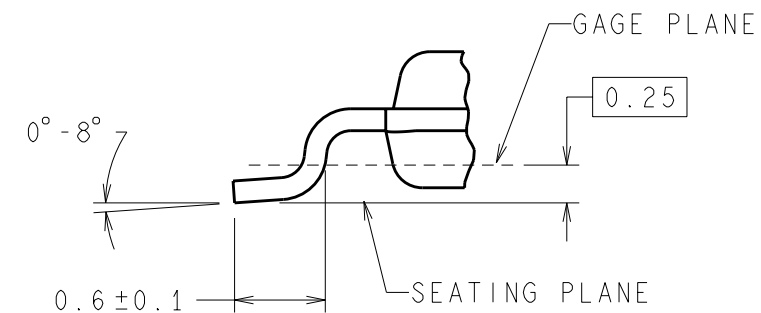
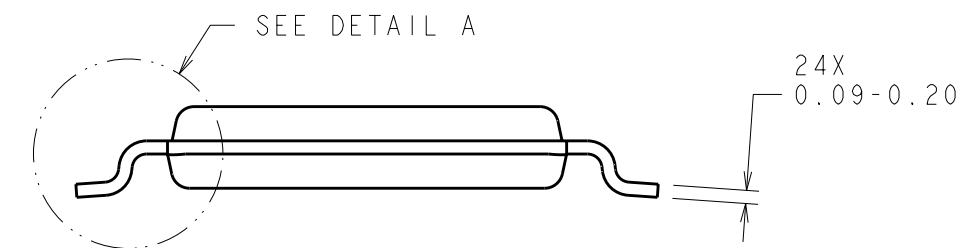
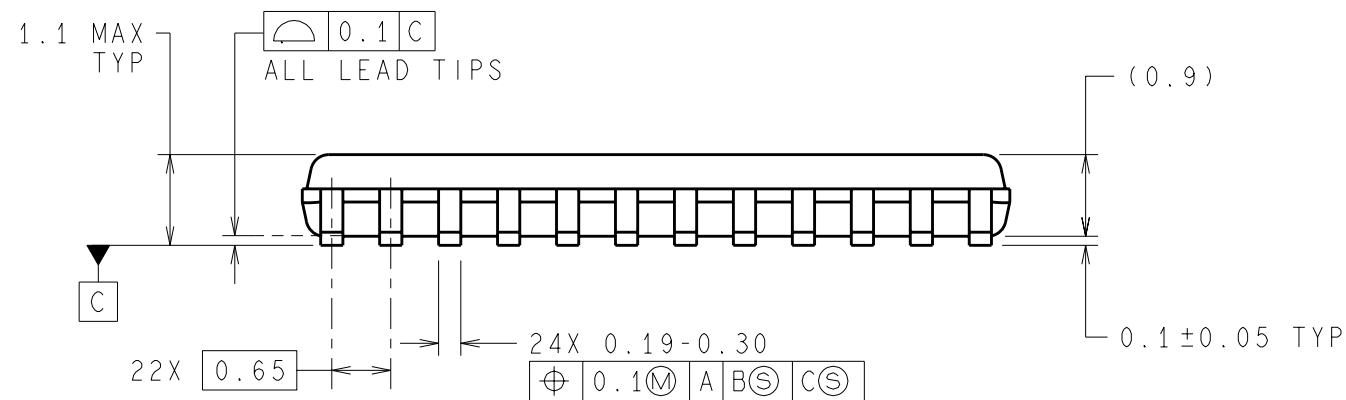


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW ON PRO/E PER CURRENT STD; CORRECT DET CALLOUT FROM D TO A.	11106	08/30/1995	MS/TC
D	LEAD POS. TOL. 0.1 WAS 0.13; CHANGE DWG FORMAT TO B SIZE; UPDATE NOTE 1; LAND PAT. DET: UPDATE TO REF DIMS.	810	11/27/2002	MS/RW
E	ADD LEAD FINISH NOTE & UPDATE TITLE.	976	03/26/2003	MS/RW



LAND PATTERN RECOMENDATION



DETAIL A TYPICAL

DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- REFERENCE JEDEC REGISTRATION MO-153, VARIATION AD.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090		
DRAWN	MARTA SUCHY	08/30/1995			
DFTG. CHK.	THANH LEQUANG	03/26/2003	MOLDED TSSOP, JEDEC, 7.8x4.4x0.9mm BODY, 24 LD, 0.65mm PITCH		
ENGR. CHK.	RANDALL WALBERG	03/26/2003			
PROJECTION	MM	SCALE	SIZE	DRAWING NUMBER	REV
		NTS	B	(SC)MKT-MTC24	E
FORMERLY: N/A				SHEET 1 of 1	