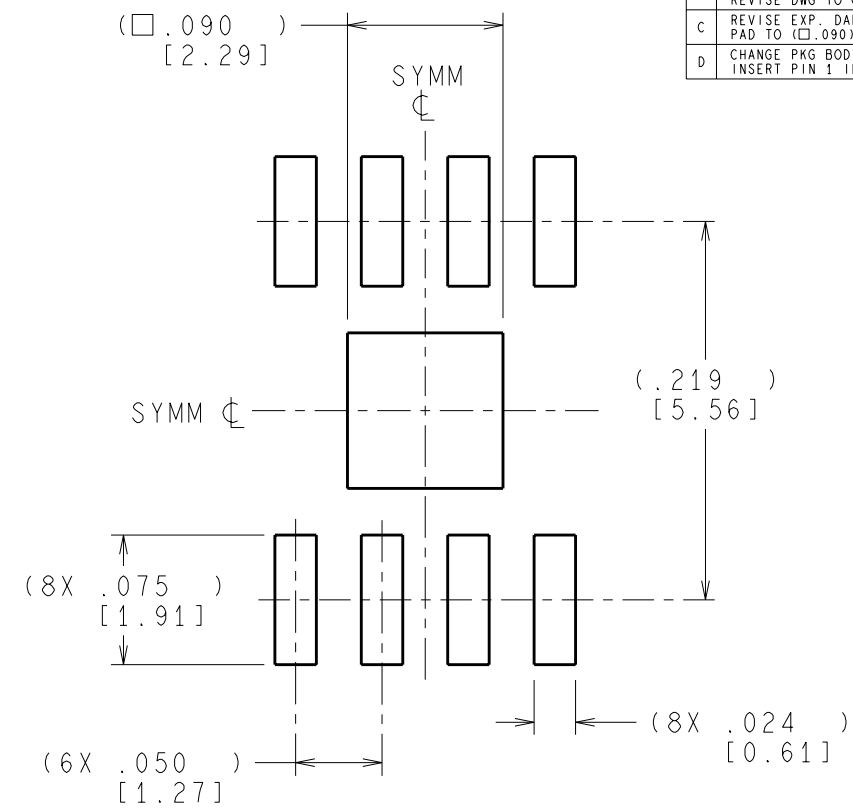
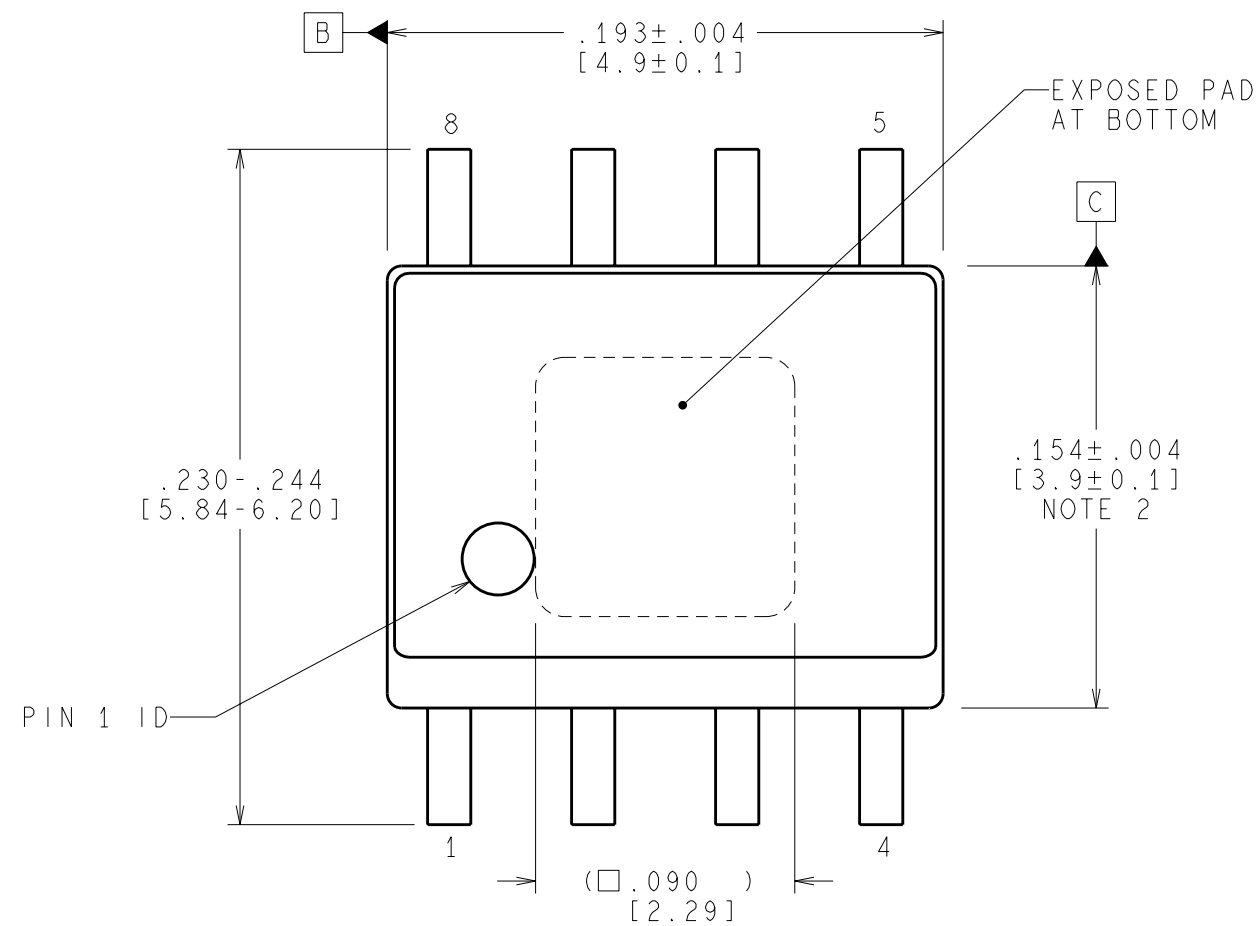
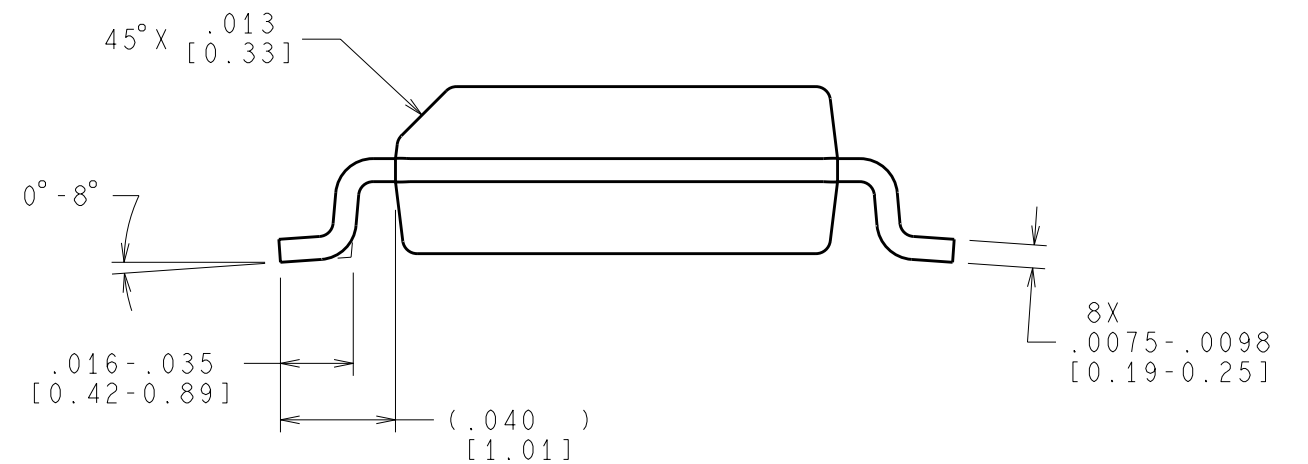
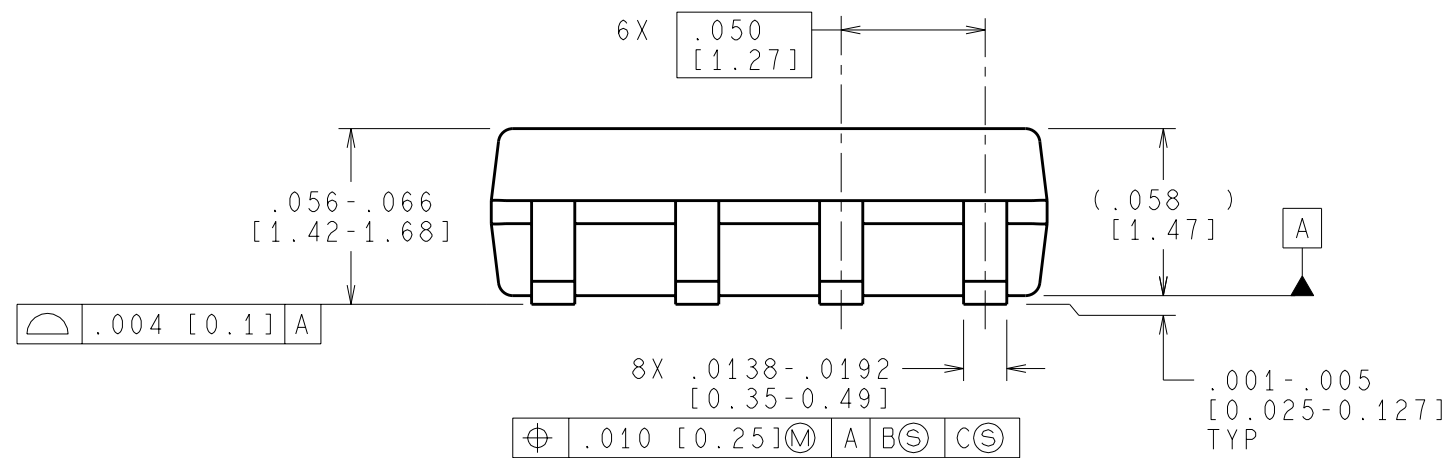


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	214	01/25/2001	MC/CD
B	REMOVE PIN 1 ID; REPLACE NOTE 1 W/ NEW SOLDER NOTE; REVISE DWG TO CURRENT STDS; CHANGE DWG FORMAT TO B	1087	06/19/2003	TL/RW
C	REVISE EXP. DAP & ADD DIM; LAND PATT; CHANGE CTR PAD TO (.090), I/O PAD LENGTH WAS (.087)	1125	07/28/2003	TL/RW
D	CHANGE PKG BODY SIZE FROM .194x.155 TO .193x.154. INSERT P1N 1 ID. REMOVE -2 FROM DRAWING TITLE.	2430	12/11/2007	MS/TL/EL



RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- DIMENSION DOES NOT INCLUDE MOLD FLASH.
- REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

APPROVALS	DATE	National Semiconductor	
DRAWN MARTA SUCHY	01/25/2001	2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DFTG. CHK. THANH LEQUANG	12/11/2007	MOLDED, PSOP, .193x.154x.058, 8 LEAD, .050 PITCH	
ENGR. CHK. EUGENE LEE	12/11/2007		
PROJECTION	SCALE	SIZE	DRAWING NUMBER
	NTS	B	(SC)MKT-MRA08A
FORMERLY: N/A	SHEET 1 of 1		REV D