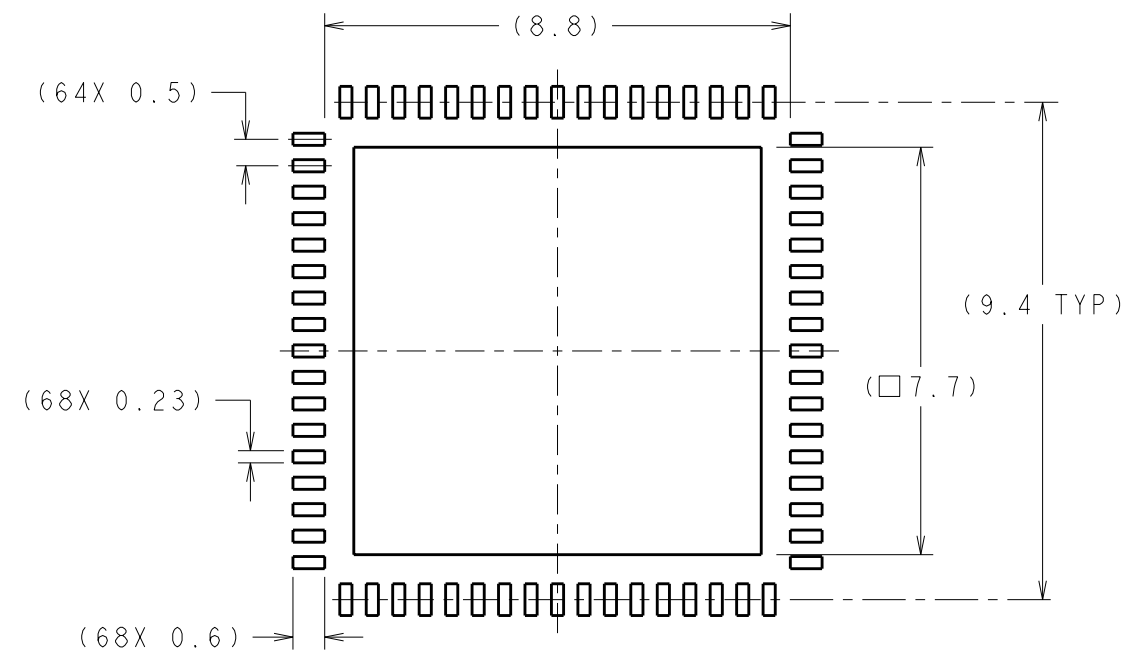
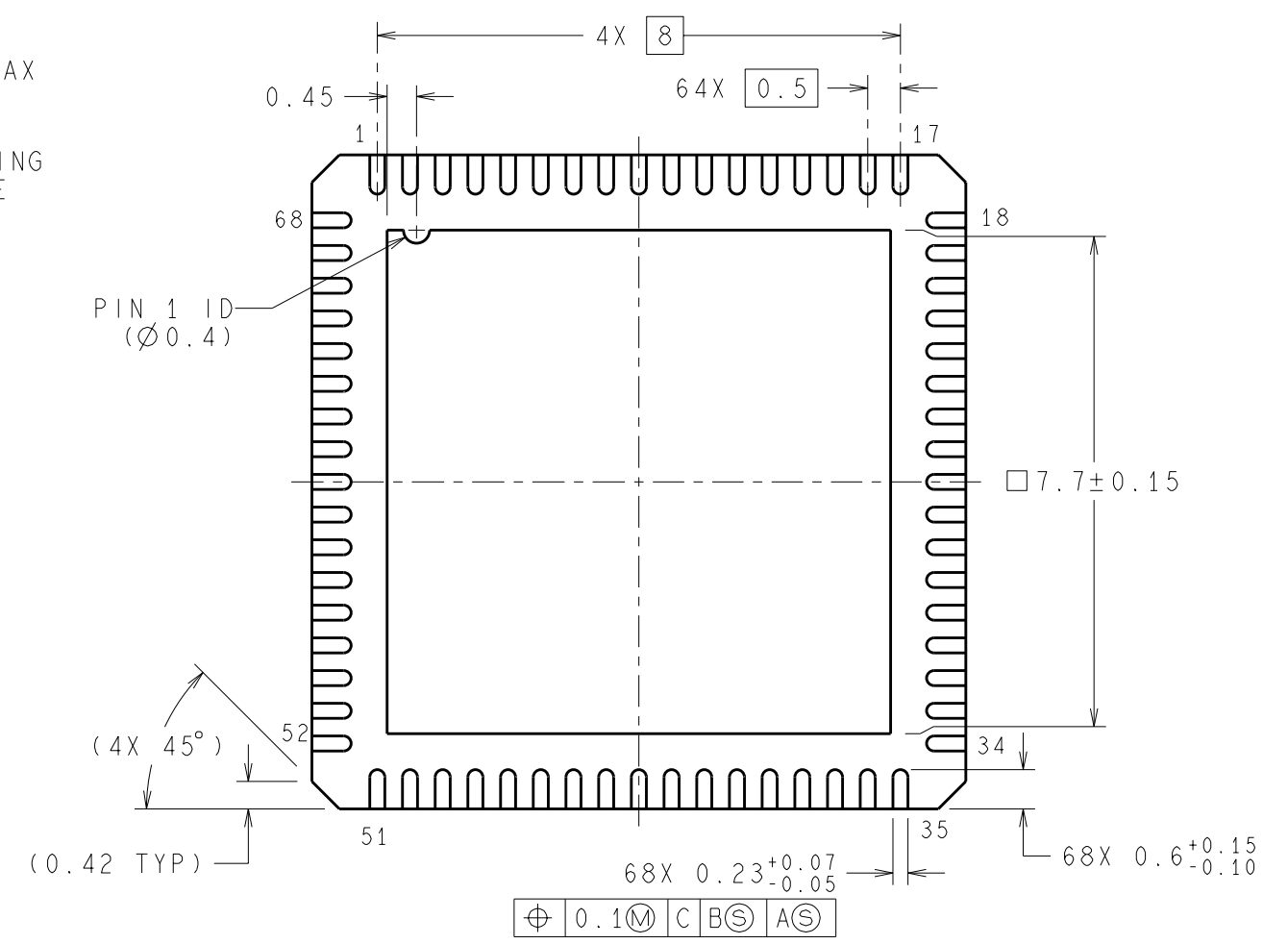
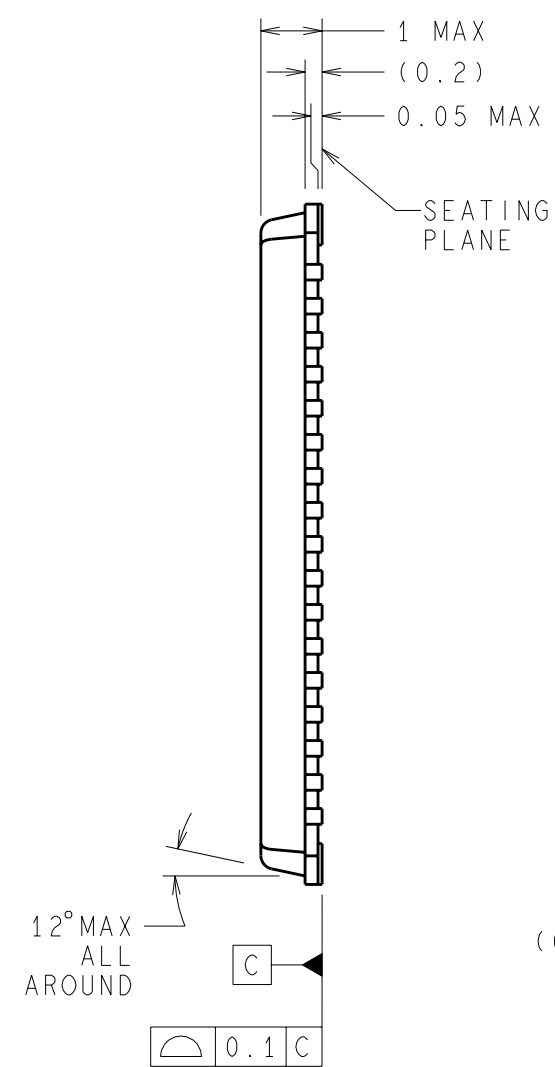
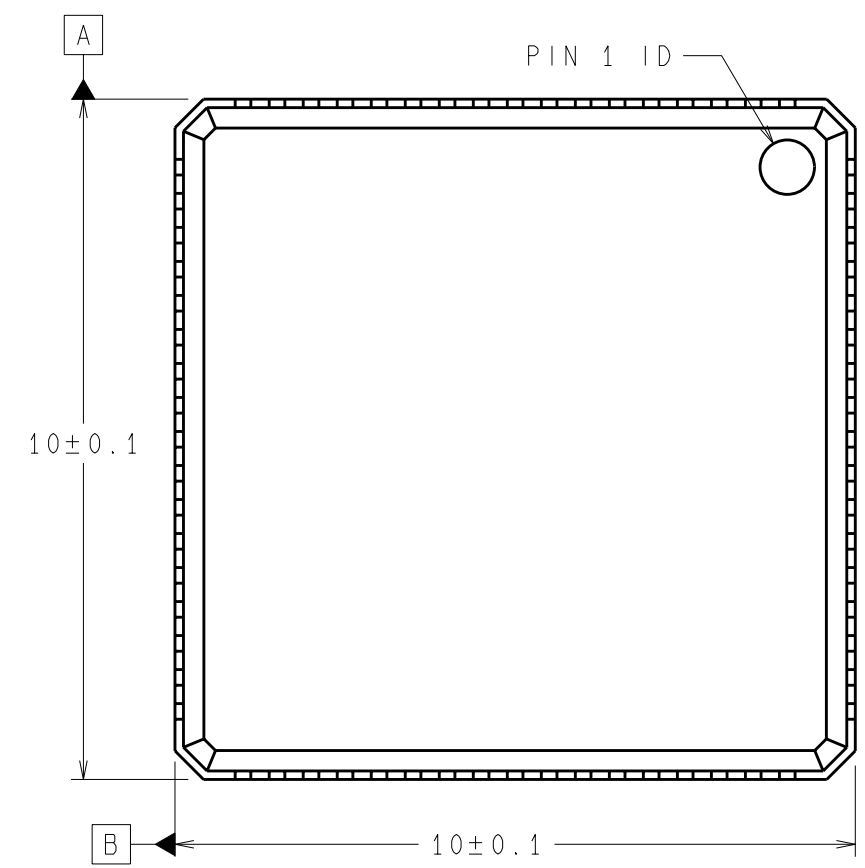


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	187	04/19/2001	TL/JS
B	REMOVE DAP SIZE TABLE; REMOVE 4 PINS AT 4 SIDES TO PACKAGE; CHANGE FROM LONG TO CIRCLED PIN 1 ID; UPDATE NOTE 1 & 2	2876	07/28/2009	EL/TKY/SL



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- REFERENCE JEDEC REGISTRATION MO-220, VARIATION VNND-2.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN T. LEQUANG		04/19/2001	
DFTG. CHK. TK Y.II		07/28/2009	
ENGR. CHK. SHAW LEE		07/28/2009	
PROJECTION:			LLP, PLASTIC, QUAD, 10x10x1mm, 68 LD, 0.5 mm PITCH
SCALE NTS	SIZE B	DRAWING NUMBER (SC)MKT-LQA68A	
FORMERLY: N/A			SHEET 1 of 1