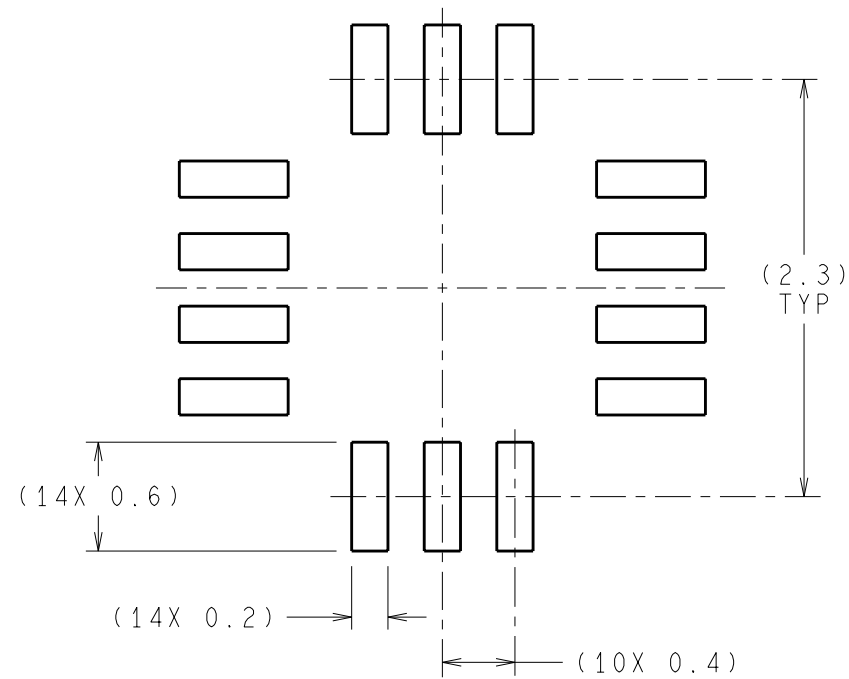
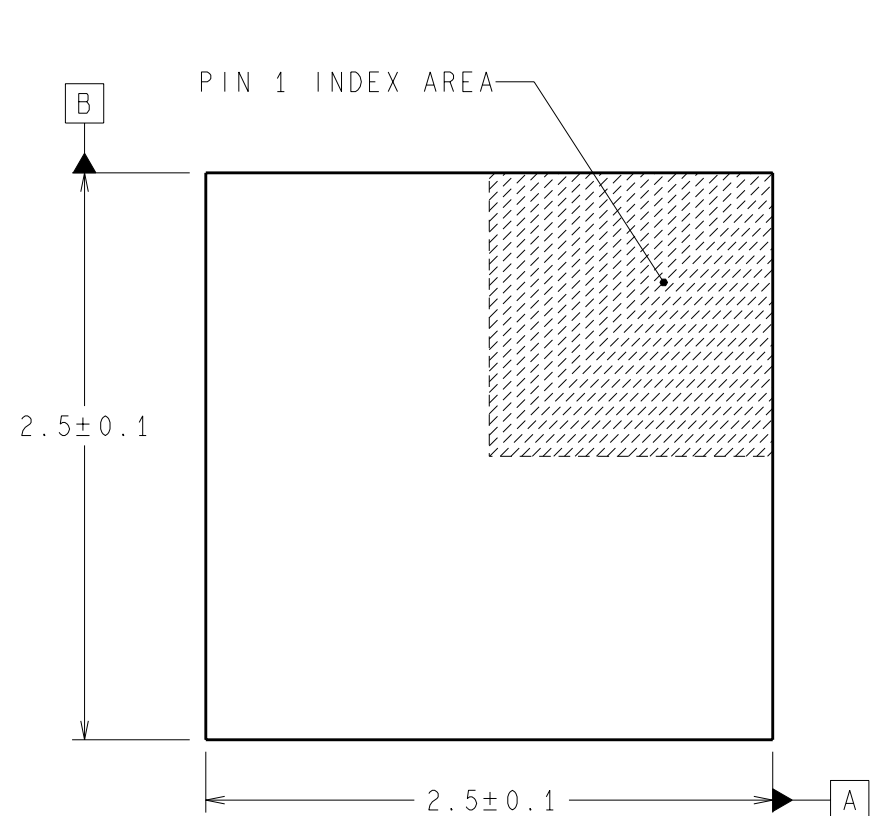


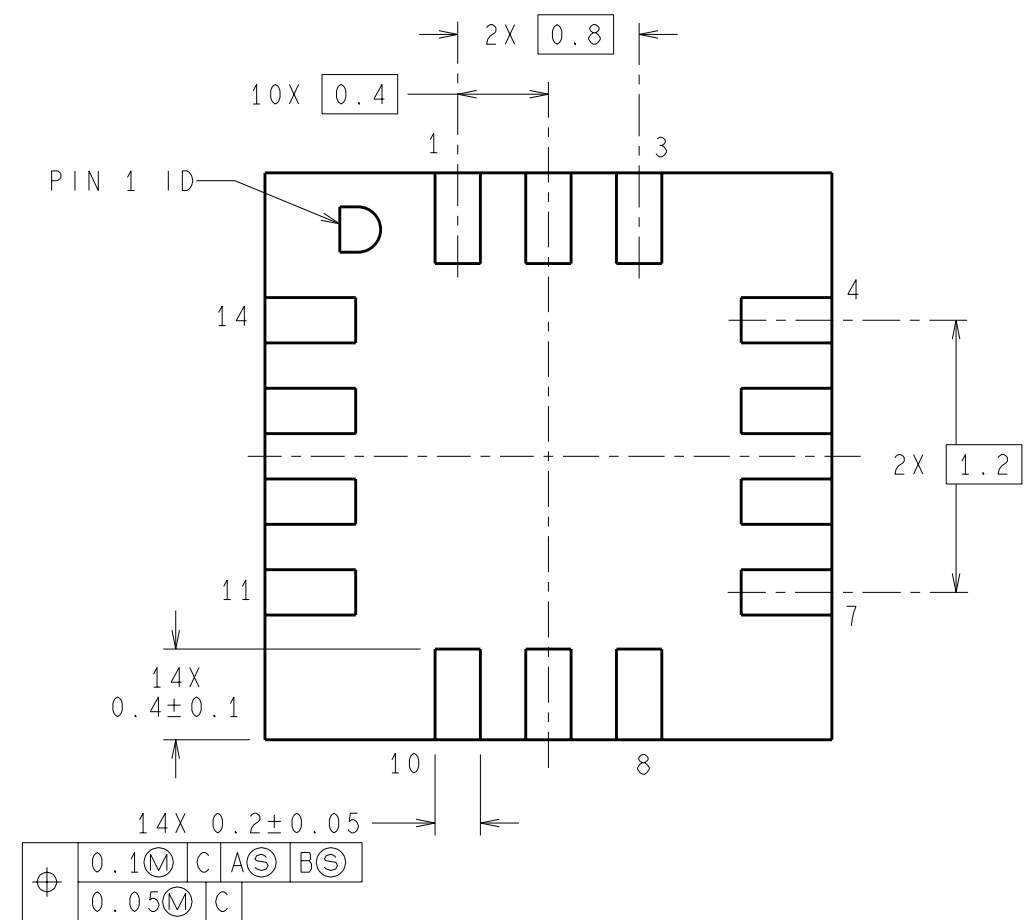
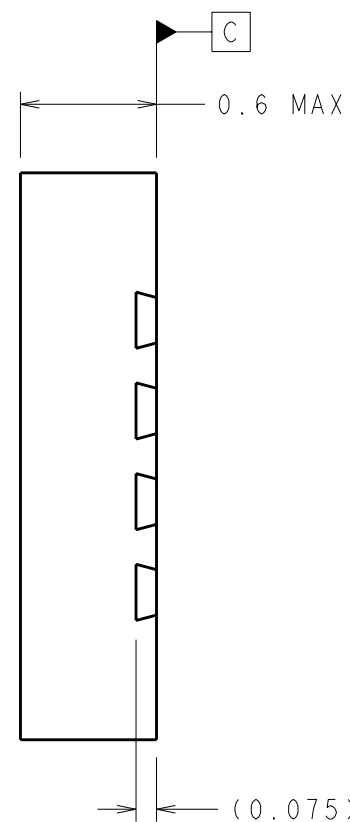
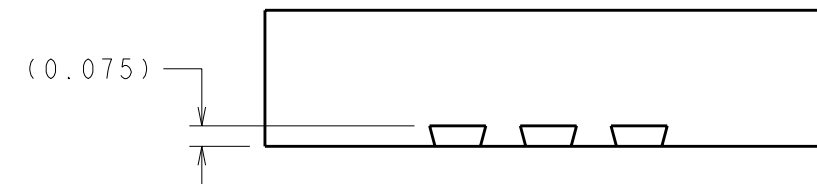
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2246	03/09/2007	TL/AT
B	REVISE DRAWING TITLE	2516	04/16/2008	TL/RW



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF APRIL 2008.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN T. LEQUANG		03/09/2007	
DFTG. CHK. KURT SINCERBOX		04/16/2008	
ENGR. CHK. RANDY WALBERG		04/16/2008	
PROJECTION: MM			LLP, 2.5x2.5x0.6mm, 14 LD, 0.4mm PITCH, NO PULLBACK
SCALE: NTS	SIZE: B	DRAWING NUMBER: (SC)MKT-LEE14A	REV: B
FORMERLY: N/A		SHEET 1 of 1	