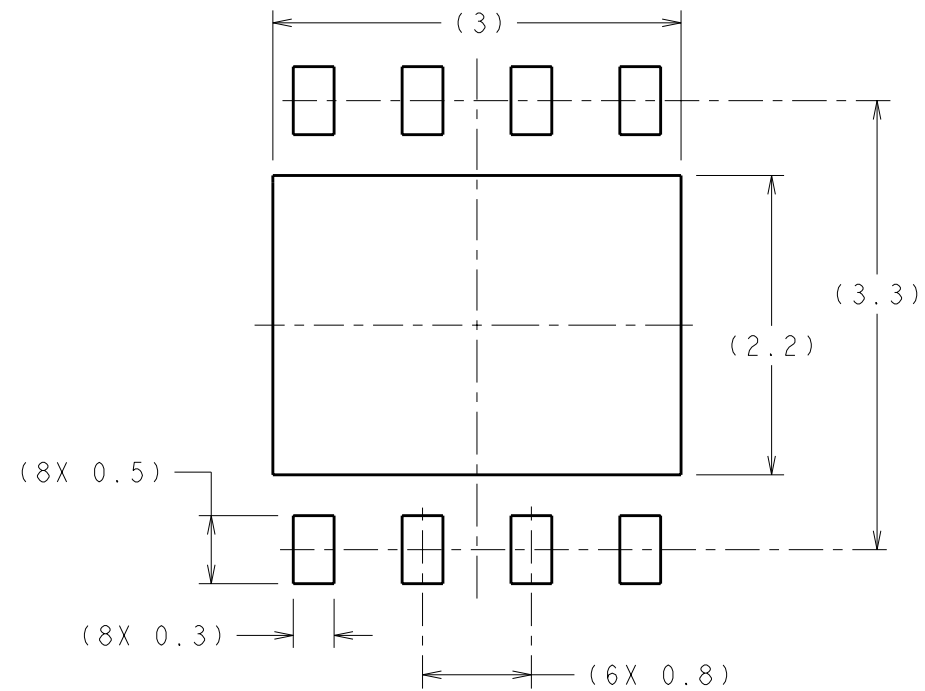
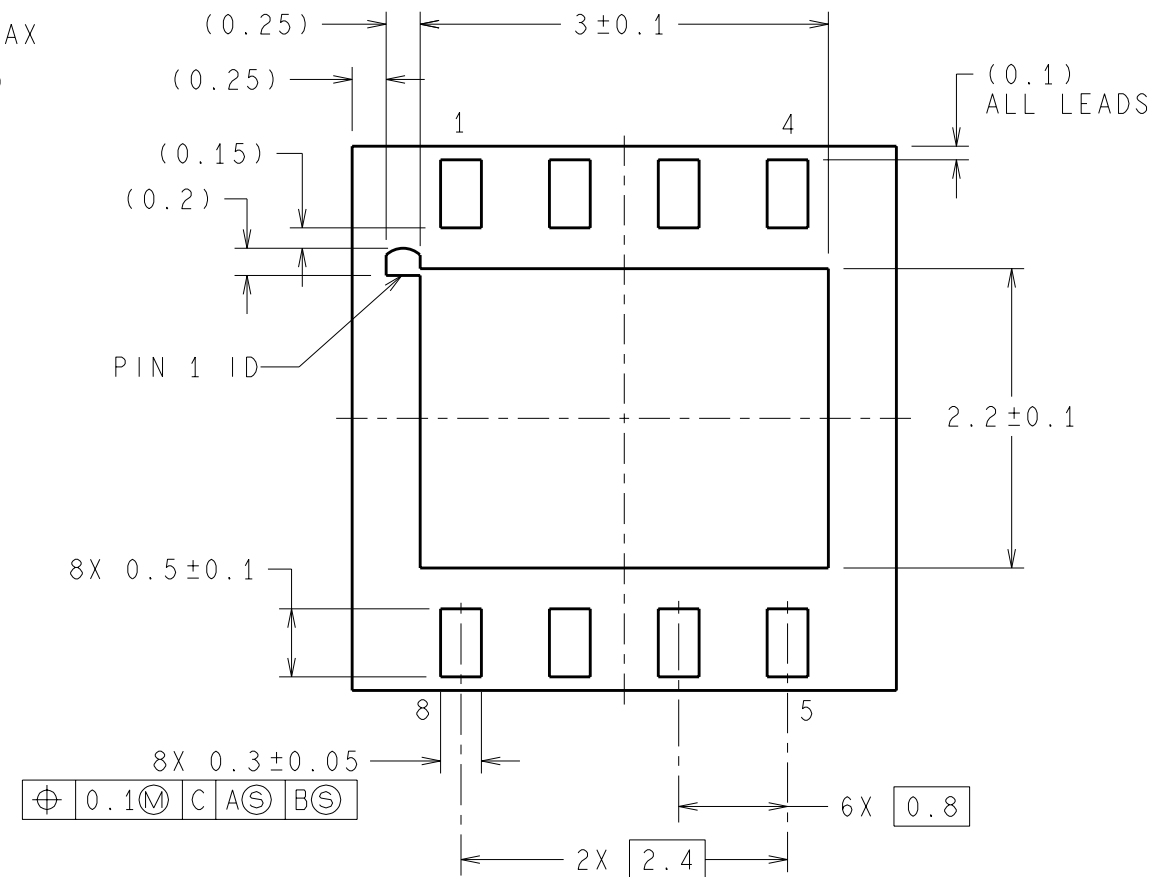
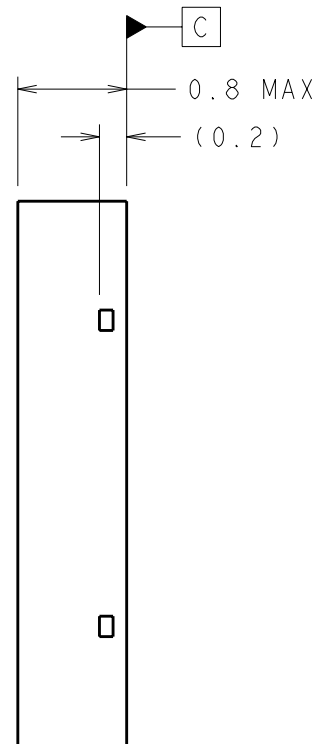
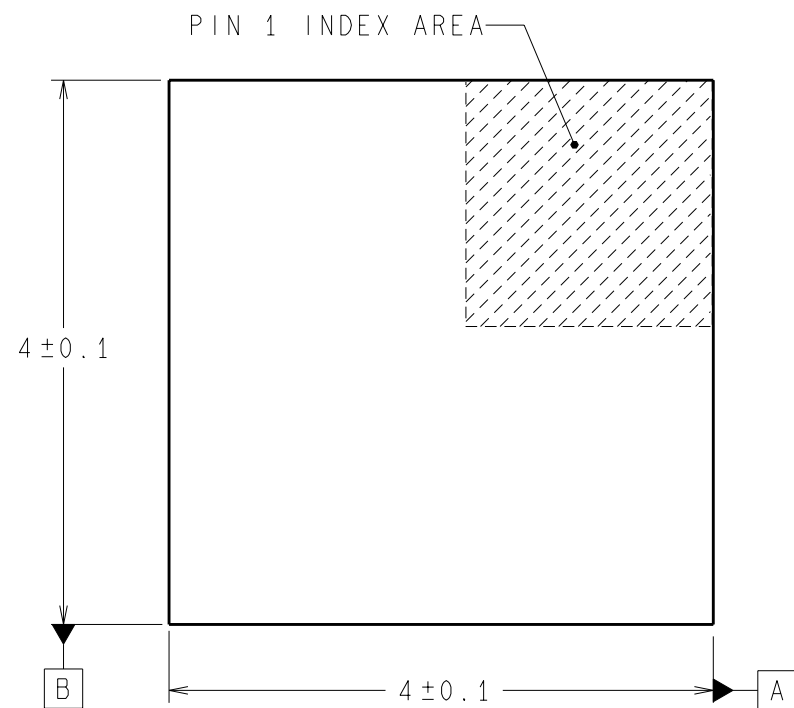


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	12443	04/27/2000	SN/TL/AL
B	REPLACE NOTE 1 W/ SOLDER NOTE; ADD PIN 1 DIM'S; UPDATE DWG PER CURRENT STD; UPDATE JEDEC NOTE (2); CHANGE DWG FORMAT TO B SIZE	1095	06/25/2003	TL/RW



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- REFERENCE JEDEC REGISTRATION MO-229, VARIATION WGGB.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN N. SANTHRAN & TL		04/27/2000	
DFTG. CHK. MARTA SUCHY		06/25/2003	
ENGR. CHK. RANDALL WALBERG		06/25/2003	
PROJECTION:			LLP, PLASTIC, DUAL, 4 X 4 X 0.75 mm BODY, 8 LD, 0.8 mm PITCH
SCALE NTS	SIZE B	DRAWING NUMBER (SC)MKT-LDC08A	
FORMERLY: N/A			SHEET 1 of 1