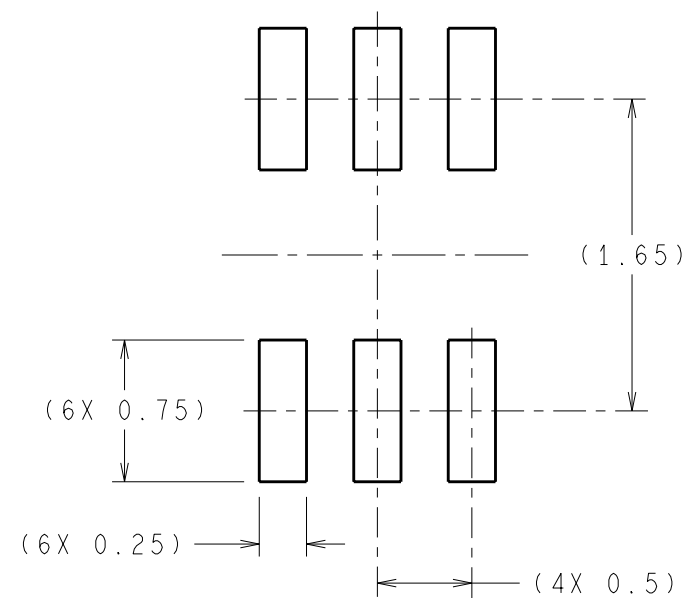
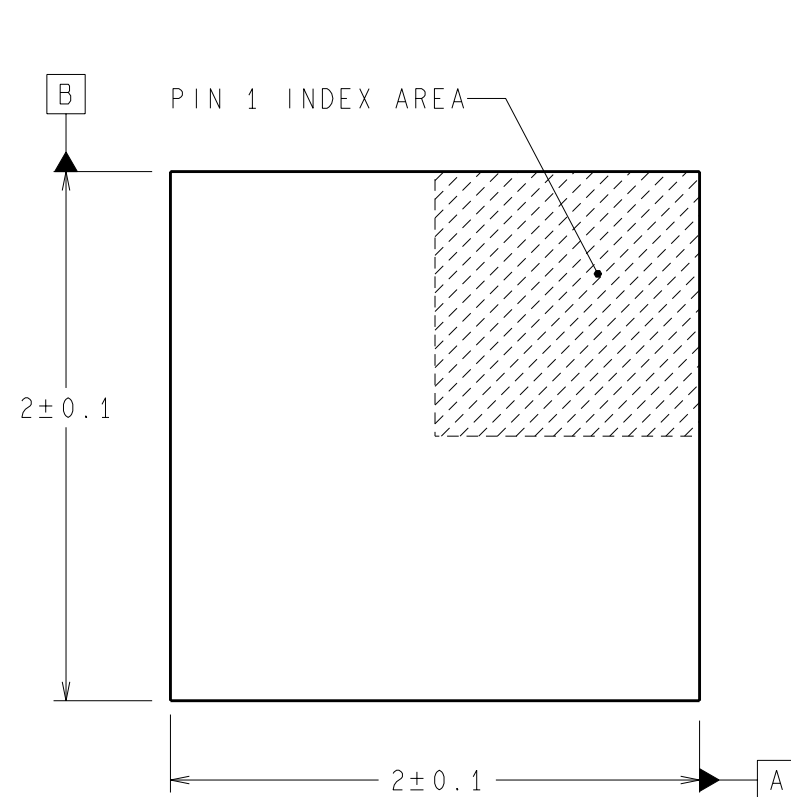


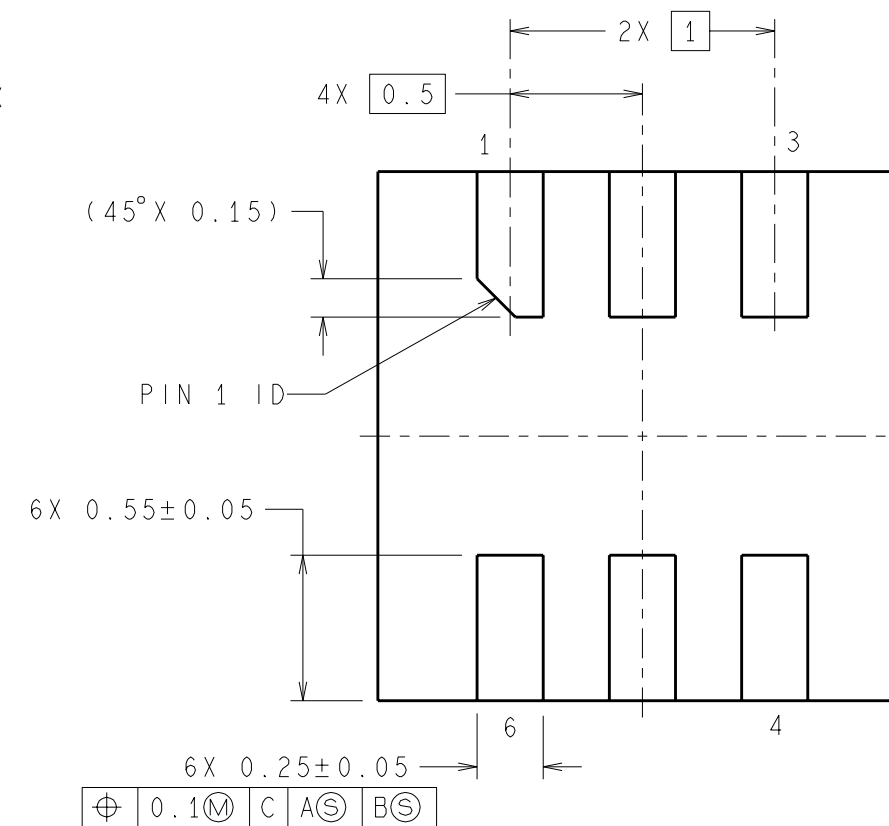
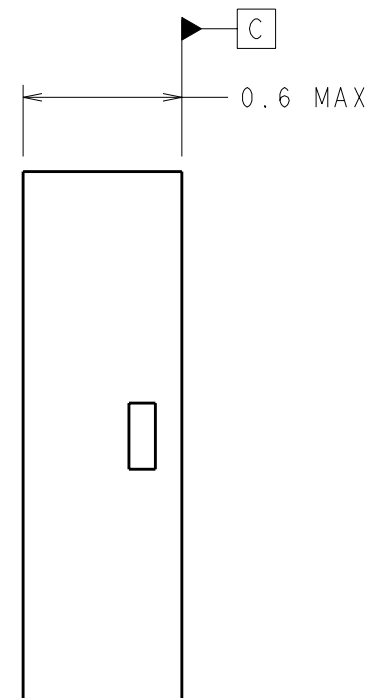
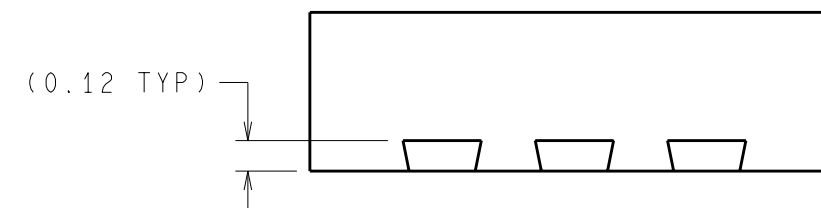
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2199	10/13/2006	TL/RW



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY



⊕	0.1(M)	C	A(S)	B(S)
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NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF OCTOBER 2006.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	T. LEQUANG	10/13/2006		
DFTG. CHK.	KURT SINCERBOX	10/13/2006	LLP COL, 2x2x0.6mm, 6 LD, 0.5mm PITCH, NO PULLBACK	
ENGR. CHK.	RANDALL WALBERG	10/13/2006		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-LCA06B	A
FORMERLY: N/A			SHEET 1 of 1	