

Effects of the Solder Oxide Layer on High Frequency Signal Propagation in Pb-Free Interconnections

Dragos Burlacu, Luu Nguyen^(*), and Jorma Kivilahti
Laboratory of Electronics Production Technology

Helsinki University of Technology
P.O. Box 3000, FIN-02150, Finland

^(*) National Semiconductor Corporation
P.O. Box 58090, Mail Stop 19-100, Santa Clara, USA

Abstract

In this paper, the effects of the surface oxide layer thickness of a Pb-free solder (Sn_{3.4}Ag_{0.8}Cu) and pure Sn on high frequency signal propagation have been investigated. To simulate the thermal effects induced by extended device powering, the Pb-free materials were annealed at 200°C for different times (up to 30 days) to increase the oxide layer thickness. The test modules consisting of lead-free microstrip lines (pure tin and SnAgCu) on a low-loss liquid crystal polymer substrate were fabricated and measured up to 50 GHz. The insertion losses of thick and native oxides were compared using transmission line theory. The results were in good agreement with the predictions, and the comparison of the insertion losses of different oxide thicknesses pointed out that the natural oxide layers induce less resistive loss than the annealed materials at microwave frequencies. It was evaluated that the resistive loss of the highly oxidized pure Sn was 0.6 dB/cm larger than that of its native oxide layer. In the case of the highly oxidized Sn_{3.4}Ag_{0.8}Cu the insertion loss was 3.5 dB/cm higher at 50 GHz as compared to that of its natural oxide.

Introduction

Interconnection and packaging technologies for high-frequency, high-speed digital and mixed signal applications are becoming ever more challenging with increasing IC functions and I/O counts, as the integration of the active components is increased simultaneously with the decrease in interconnection dimensions. New applications demands are pushing up the communication frequencies towards 50 GHz and the digital clock rate beyond 5 GHz [1]. With the frequency increase and bump size scaling down, the reliability of the interconnections and signal integrity issues are becoming more demanding at the component/board level. The parasitic effects such as signal reflections, delay, dispersion, crosstalk, ground bounce and voltage drop must be well controlled to ensure good performance of devices.

Careful consideration should be paid not only to the interconnection design but also to materials and assembly process solutions to meet the signal integrity demands and faultless device operations. A good understanding of high frequency signal transmission in lead-free solder interconnects will become important, as the July 1, 2006 WEEE Directive deadline for lead-free implementation approaches. Until now, research on Pb-free solder materials were carried out mainly to investigate the reliability issues

and to determine the DC performances. Research of the RF characteristics of the Pb-free interconnections and insertion losses measurements were not known to us.

The high operational frequencies lead to the augmentation of resistive losses at interconnection sites as the skin effect prevents the current from penetrating deep into the metal. Thus, the current flow is limited to a very small area on the outer surface of the conductor that decreases with the frequency increase [2]. The skin effect, together with the roughness, and bump shape could increase further the resistive loss at the interconnection [3].

Furthermore, the increased temperature of the new generation of components due to the higher number of functions performed by the ICs increases the signal integrity concerns as the high temperature produce favorable conditions for further oxide layer growth on the surface of the solder bump [4]. Moreover, the presence of the thick oxide layers together with the skin effect is becoming a concern for the high frequency signals integrity as the current penetration depth is lowered to 0.745 μm at 50 GHz.

The effect of thick oxide on the bump surface resembles the effect of high resistivity metal layers deposited on the outer surface of metals described by Denlinger *et al.* [5]. In that study, it was demonstrated that thick layers of higher resistivity materials deposited on the surface of the conductor increase the resistive loss from 30 to 50 %, as a high ratio of the power flow is conducted through the outer deposited materials.

In this paper, for the first time the effect of oxide layers grown on Pb-free interconnections on signal integrity frequencies up to 50 GHz are analyzed. The research will be carried out with the help of the transmission line theory and of specially designed, fabricated and measured test boards. The insertion loss of several hundred bumps will be simulated with good accuracy by fabricating the transmission line out of the Pb-free materials. Thus, the inherent errors present in the interconnection losses analysis will be avoided and the measured results of the longer transmission line will be more accurate.

Design and Materials

High frequency measurements up to 50 GHz required special consideration for the concurrent design, manufacturing, and measurement. To evaluate and compare the influence of oxide layers on insertion loss of the high-speed signals propagation, prototype boards were designed,

manufactured and measured up to 50 GHz. The high frequency research required special considerations from the design, manufacturing, and measurements as all three issues were addressed concurrently. Utilizing transmission line theory, it was possible to determine the values of resistive loss introduced by the skin effect when a thick oxide layer was present on the conductor surface. A 4 cm transmission line was manufactured out of Pb-free materials to simulate the effect of a few hundred solder balls. The substrates for all samples were manufactured from the same materials and with the same process parameters. Thus, dielectric, radiation, and surface wave power losses were the same for all boards. Measuring the total power losses of the test coupons, the values of attenuation due to conductor loss induced by the oxide layer thickness could be determined by comparing the measured results of the samples with natural oxide (NO) with the ones of the highly oxidized (HO) samples. The difference between HO and NO results indicate the value of the resistive loss introduced by the oxide presence because NO insertion loss includes all transmission line losses (1) of the materials with native oxide [3].

$$\alpha_T = \alpha_c + \alpha_d + \alpha_r + \alpha_{sw} \quad (1)$$

with α_T – attenuation due to total losses, α_c – attenuation due to conductor loss, α_d – attenuation due to dielectric dissipation loss, α_r – attenuation due to radiation loss, and α_{sw} – attenuation due to surface-wave propagation loss.

The test board consisted of two parts, the carrier substrate and the Pb-free material under investigation (Fig. 1).

The material for the carrier substrates used in this research, the liquid crystal polymer (LCP), was selected considering its electrical parameters stability over a broad band of microwave frequencies, dielectric constant (ϵ_r) = 3 and loss tangent ($\tan \delta$) = 0.003 [6]. Furthermore, by using thin substrates of 125 μm , the multiple modes wave propagation in the dielectric at high frequencies was avoided. Thus, the transmission line de-tuning was kept to a minimum, and high frequency dielectric loss was decreased. This was possible as the LCP material accounts for about 80 % percent of the dielectric materials used for the boards. The presence of the epoxy glue and little information on its electrical parameters led us to simulate it as an epoxy polymer having a dielectric constant of 3 considering the mean value of several commercial epoxy glues without fillers.

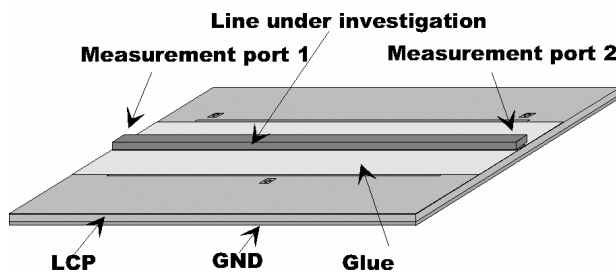


Fig. 1 – Schematic presentation of the test board.

The Pb-free materials under investigation were pure tin (Sn) and the lead-free solder composition (Sn3.4Ag0.8Cu) (SnAgCu for short). The SnAgCu material was cold rolled

down to a thickness of 100 μm , while pure Sn 99.999 was provided by Goodfellows Inc. To simulate the long term thermal effects induced by hot running components, the materials were annealed at 200°C for 30 days to create a thick oxide layer.

The dimensions of the microstrip line were calculated utilizing the line calculator from Agilent – Advanced Design Systems software to meet the 50 Ω characteristic impedances required by the measurement system. Nevertheless, due to manufacturing issues raised by the small width of the required line, the thick sheet of Pb-free materials, and the poor adhesion of the sacrificial polymer to the metals, the line dimensions could not meet the 50 Ω requirements. A compromise solution was adopted, and a 45 Ω characteristic impedance microstrip line was used instead. The change did not affect the investigation outcome since the evaluation was carried out using the insertion loss parameters. Finally, the microstrip transmission lines with the width of 450 μm were successfully manufactured for all samples.

Manufacturing of the test boards

The test boards were fabricated using a subtractive process. The detailed scheme of the manufacturing process is presented in Fig 2. First, the Cu foil present on the top of the substrate was patterned to create the alignment points for the transmission line as this must make a 90° angle with the measurement device. The fabrication was completed using subtractive photolithographic process (Fig. 2.a). Then, the pure Sn and the SnAgCu sheets were attached to the carrier substrate by utilizing an epoxy adhesive. The adhesive thickness had to be same for all the samples so that the RF-parameters are the same for all test boards. For this, two sheets of polyimide tapes were applied to the substrate edges to supply the height reference for the applicator (Fig. 2.b). The adhesive was spread over the area by having as a reference point for aligning the tapes (Fig. 2.c). After the adhesive had been applied, the metal sheet under investigation was attached to the carrier substrate and the assembly was passed through the laminator heated at 75° C, and set to the highest pressure to eliminate air bubbles trapped between the metals and substrates (Fig. 2.d). Finally, the line dimensions were adjusted to the required target by utilizing the high-resolution lithography process available in the laboratory. A 30 μm thick sacrificial layer of AZ 4500 from Clariant GmbH, was spun, exposed, and developed (Fig. 2.d). The patterned artwork was designed considering the under-etch previously determined for each material that varied from 100 μm in case of NO pure tin to 300 μm for SnAgCu HO. Lastly, the metal sheets were patterned and etched to the required width to meet the 45 Ω requirements (Fig. 2.f).

After processing, the test boards were microscopically inspected under a microscope to ensure that there was no damage, and the dimensions matched with the design documentation (Fig. 3). More information on the process accuracy was collected from the cross-sectional samples made from the measured boards. However, some anomalies were found and appeared to be dependent on the etching process as it was influenced by the oxide layer formation and the orientation of the Sn grains.

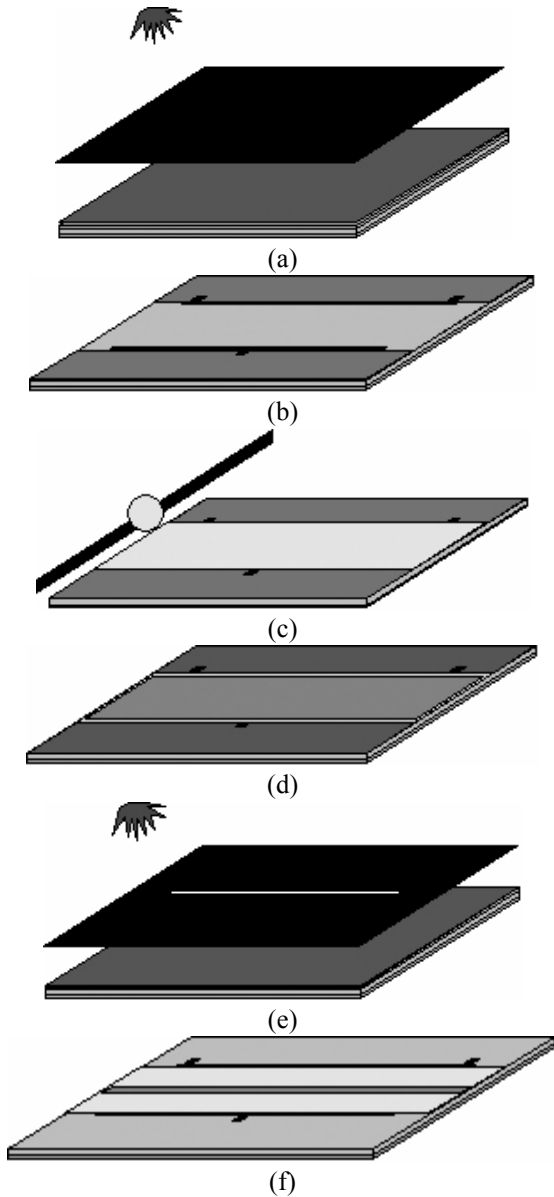


Fig. 2 – Schematic presentation of the manufacturing process.

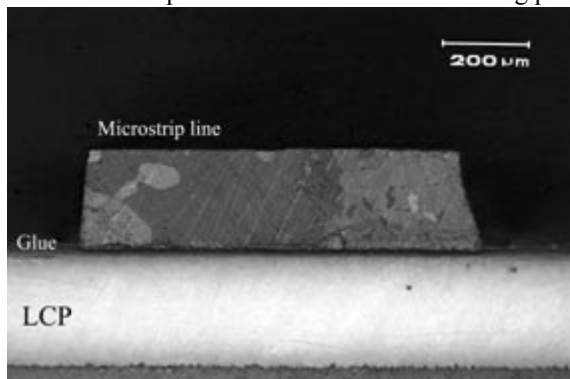


Fig. 3 – Cross section of a pure Sn test board.

Electrical Measurements

Electrical measurements were conducted from 500 MHz to 50 GHz with the help of an HP8510C vector network analyzer (VNA) used to collect full, two-port S-parameters. The test samples were the microstrip transmission lines with 45 Ω characteristic impedance. The VNA connection to the

test coupons was realized with the help of the universal test fixture (UTF) 3680 from Anritsu.

The test method consisted of system calibration, test apparatus, circuit validation, and electrical data collection. The measurement system was calibrated using a TRL calibration technique performed with the help of the microstrip calibration kit 36804-10M from Anritsu. Utilizing this calibration, the measurement reference of the ports was shifted from the connector point at 5 mm inside the sample from each port. As a result the insertion loss measurement was performed for only 3 cm of line. Each test specimen was mounted in a UTF and the S-parameters were measured for 401 points for the frequency range under investigation.

Results and Discussion

The comparison of the insertion losses of the Pb-free material under investigation was carried out with the help of the insertion losses (S_{21}) evaluation of each material and condition. After the measurement, the results were mathematically manipulated so that the insertion loss per unit length was obtained as a function of frequency. The insertion loss was calculated with the help of the Matlab program where the measured results were divided by the total length of the transmission line (2) [7].

$$InsertionLoss = 20 * \log \left(\sqrt{(S_{21real})^2 + (S_{21img})^2} \right) / 3 \left[\frac{dB}{cm} \right] \quad (2)$$

The repeatability of the test coupons was a key point in this study as it was assumed that the dielectric, radiation and surface wave losses were the same for all the manufactured test boards. The measured results showed a low value dispersion as the standard deviation of electrical characteristics of the transmission lines was calculated [8] (3) to be $\sigma = 0.217$ for an average value $x = 2.91$ at 36.3 GHz.

$$\sigma = \sqrt{\frac{\sum_{i=0}^{n-1} (x_i - \bar{x})^2}{n-1}} \quad (3)$$

The maximum value of 7.45% percent deviation was very good considering the noise figure present in the measurement results (Fig. 4).

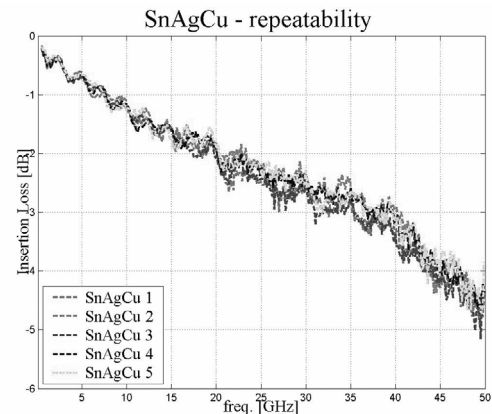


Fig. 4 – Repeatability of the insertion loss SnAgCu test boards.

Comparing the pure Sn and SnAgCu samples insertion losses up to 50 GHz, it was noticed that the two materials had similar values for the insertion losses up to 45 GHz (Fig 5.). The result suited the predictions, as the presence of Sn in the SnAgCu alloy account for about 95.8 %wt, and the only difference was the microstructures of the materials.

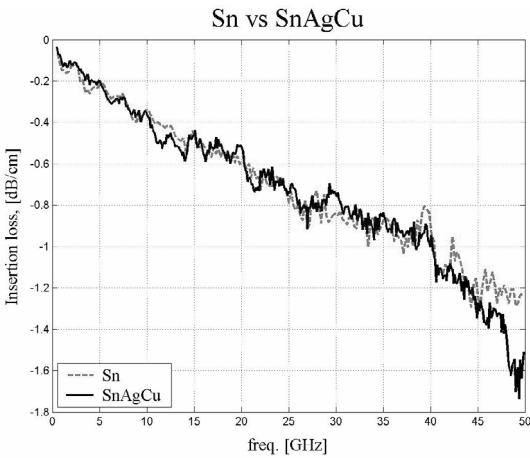


Fig. 5 – Comparison of insertion losses between Sn and SnAgCu test boards.

Nevertheless, an increase in the losses was noticed from 45 to 50 GHz. Investigation on the SnAgCu material showed that this difference could be due to the presence of manufacturing impurities on the surface of the material or to higher roughness. The latter corroborated the fact that the skin effect led to increased losses. The possibility of residues present on the surface of the alloy will be discussed later on in the paper.

The comparison between the electrical performances of the NO and HO Sn samples (Fig. 6) showed that the Sn HO samples had higher insertion losses than Sn NO ones. The largest difference, encountered at 50 GHz, was about 0.6 dB/cm and represents an increase of 50% in the insertion losses compared to the Sn NO.

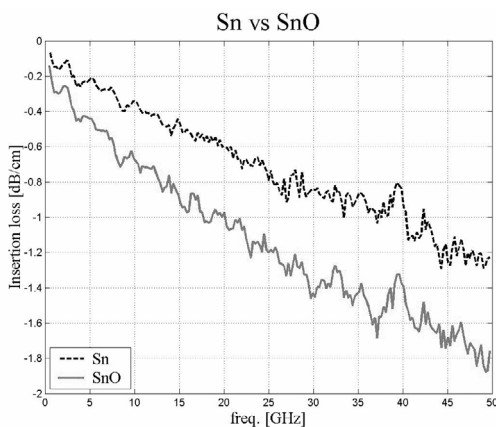


Fig. 6 – Comparison of insertion loss between Sn and SnAgCu test boards.

Furthermore, the presence of the high loss layer on the outer surface of the conductor was noticed, as from 2 to 25 GHz the SnO loci shows a slight parabolic increase of losses corresponding to the added loss by the skin effect in the high resistivity layer. Moreover, the oxide layer presence could be

highlighted by comparing the resonant frequencies of Sn and SnO results. A shift of about 1 GHz was noticed, representing the capacitive loading introduced by contact between the board and the UTF connector on the resonant circuit of the transmission line.

Insertion loss comparison of the annealed samples of SnAgCu and the ones with natural oxide (Fig. 7) showed that the HO samples were very lossy. The maximum value of the insertion loss of HO was 5.2 dB/cm at 50 GHz creating a difference of 3.5 dB/cm between materials loss – about three times larger than the one of the NO samples. A slight shape of parabolic increase of losses could be noticed from 2 to 25 GHz due to added resistive loss by the skin effect.

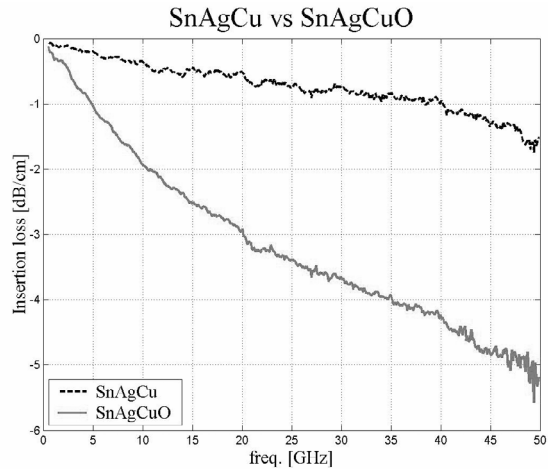


Fig. 7 – Comparison of insertion loss between Sn and SnAgCu test boards.

Higher losses were anticipated from the early stages in the manufacturing process. First, it was noticed that the line dimensions were difficult to control as the under-etch depended on the Sn grain position in the material as this were large enough to create a very uneven width for the transmission line. Furthermore, the etching time of the samples was measured to be two times larger than in the case of pure Sn HO. This indicated that on the material surface, a protective layer thick enough to effectively prevent the material etch was formed. After manufacturing, during microscopic inspection, a thin layer of residues in the conductor proximity was noticed (Fig. 8). This was present only where under-etch occurred, namely, in the region protected by the artwork – in this case for about 150 μm on each side.

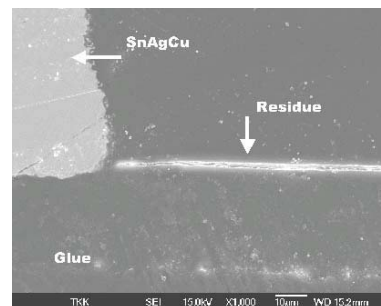


Fig. 8 – Cross-sectional SEM image exhibiting thin layer of residue nest to a transmission line.

Further analysis of the cross samples from SnAgCu HO transmission lines was carried out with the help of Field Emission Scanning Electro Microscope (FESEM) and Electron Dispersive Spectroscopy (EDS). Using these techniques, it was possible to identify tin, oxygen, and sulphur as the composition of the residues. The same composition was also found on the analysis of the conductor outer layer with both FESEM/ESD and optical inspection. Thus, the hypothesis of samples contamination from the etching bath was eliminated. The layer containing sulphur was encountered only on the annealed samples of SnAgCu (Fig. 9).

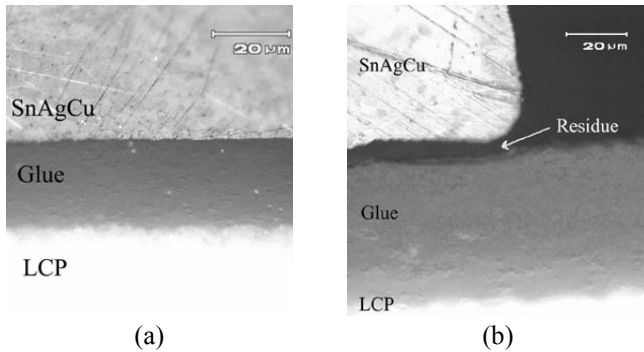


Fig. 9 – Optical micrograph showing cross-sectional structure of the transmission line in the case of SnAgCu NO (a) and SnAgCu HO (b) samples.

The formation of the layer containing sulphur was enabled by the presence of Cu and Ag in the alloy composition. One possible source of sulphur was the atmosphere since the annealing was performed in atmospheric air. Further investigation will be carried out to determine other possible sources of sulphur.

Considering the presence of the residues on the test samples, further investigation was required to determine its influence on the measurements results. Analysis of the reflection parameters (S_{11}) of the measured samples was performed. The measured data showed that the results correspond to the 45 Ω impedance line. Nevertheless, the oxide presence caused a slight mismatch by detuning the transmission line when it was compared to the SnAgCu NO parameters (Fig. 10).

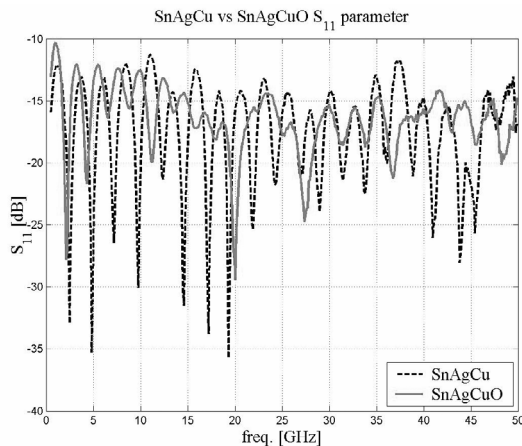


Fig. 10 – Comparison of reflection parameters (S_{11}) for SnAgCu NO and SnAgCu HO.

Thus, the residues presence in the high insertion loss from the conductor was overruled as it was proven that the power flow was mainly in the metal under investigation. As in the case of Sn, the presence of the oxide on the surface of the material could be noticed as the resonant frequency is slightly shifted with 1.5 GHz comparing the S_{11} parameters of SnAgCu HO and NO samples.

To determine the oxide layer thickness for both HO and NO, test coupons taken from the metals sheets were analyzed using the Sequential Electrochemical Reduction Analysis – Surface analysis (SERA) measurements. The calculation of the thickness of the oxide layers of the samples was based on the following potential thresholds for Sn from -0.75 to 1.06 V and for (SnO_2) from -0.106 to -1.1 V. The mean values of the thickness of stannous oxide (SnO) and stannic oxide (SnO_2) measured from three samples are presented and the standard deviation was calculated to be 22% (Table 1).

Material	SnO [\AA]	SnO ₂ [\AA]
Sn	45	50
SnO	225	130
SnAgCu	40	Not detected
SnAgCuO	Not detected	Not detected

Table 1 – Measured thickness of oxide layers.

Further investigation regarding the absence of stannic oxide for the SnAgCu samples with natural grown oxide and on the long term oxidation of the alloy will be carried out.

Conclusions

The investigation of the insertion losses of the surface oxide layer thickness on a lead-free solder composition (Sn3.4Ag0.8Cu) and pure Sn on high-frequency signal propagation was carried from 500 MHz to 50 GHz. The results of electrical measurements proved that the process repeatability was good and manufacturing accuracy met the theoretical requirements. In the case of SnAgCu samples the maximum standard deviation was $\sigma = 0.217$ for an average value $x = 2.91$ having 7.45% percent standard deviation. The comparison of the insertion losses of the Sn and SnAgCu samples with natural oxide showed similar properties up to 45 GHz, which depended on the high Sn content of the samples as the presence of Sn in the SnAgCu alloy is about 95.8 %wt.

The analysis of the oxide layers' influence on the resistive losses of pure Sn showed that the highly oxidized samples had higher insertion losses than the ones with native oxide layer – the difference increasing up to 0.6 dB/cm at 50 GHz. The insertion loss for the highly oxidized SnAgCu samples was very large. At 50 GHz, the difference between such samples and the ones with natural oxide increased up to 3.5 dB/cm. It was detected that the increased insertion loss values were caused by sulphur contamination on the outer surface of the conductor. By analyzing the reflection parameters of the highly oxidized SnAgCu samples, it was shown that the residues present in the vicinity of the line did not affect the insertion loss. The effect noticed was a slight detuning of the transmission line. Further research will be carried out to determine the oxide formation on the Pb-free material.

The results of this study indicated that the influence of the oxide layer of Pb-free (Sn_{3.4}Ag_{0.8}Cu and pure Sn) materials is important, especially when the formation of thick oxide layers on solder bumps is accelerated by temperature rise. The increased insertion loss due to thick oxide layers formation can raise signal integrity concerns. The SERA measurements of the oxide layer thickness indicated that the oxide layer of pure tin is about 0.035 μm thick, whereas the penetration depth is 0.745 μm .

Acknowledgments

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