

Solder Joint Reliability Model with Modified Darveaux's Equations for the micro SMD Wafer Level-Chip Scale Package Family

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Abstract

Historically, energy-based solder fatigue life models have been used primarily for PBGA or similar package configurations. In this paper, we extend the energy-based method to newly emerged Wafer Level, Chip Scale Package (WL-CSP). National Semiconductor's micro SMD package family was chosen as the test vehicle. Among all energy-based methods, Darveaux's model is arguably the most popular one due to its well-documented good correlation with the actual tests. To maintain consistency in results, Darveaux suggested that the solder joint be meshed such that the element size in its height direction has fixed value. However, we found in our study that Darveaux's model faired poorly in capturing the package fatigue life, even though the mesh size issue was carefully addressed. In view of the drastic difference in solder ball size between WL-CSP and PBGA, on which Darveaux's model is based, we argue that in addition to the element size in the solder height direction, the finite element calculation of inelastic dissipation may also depend on other meshing parameters, which may vary depending on the specific geometry of the solder bump. Consequently, we proposed a revised empirical equation to calculate the package fatigue life for micro SMD. The new equation is derived from correlating the simulation results with the test data. We also demonstrated that the new equation was capable of achieving a similar accuracy level as compared with Darveaux's model for PBGA packages. The study also provided for the first time a good parametric model scalable to larger micro SMD I/O count. In addition, the impact of different modeling schemes was also evaluated in terms of their accuracy and efficiency.

Introduction

Solder joints are widely used in the electronic packaging industry to provide electrical, thermal, and mechanical connections between the package and the Printed Circuit Board (PCB). One of the common solder failures is the formation of fatigue crack at the solder-package interface under cyclic thermal loading. The growth of the crack will eventually cause the failure of the package. How to accurately predict solder joint fatigue failure without resorting to the rather lengthy and costly tests has always been the concern of every IC company. It remains as a formidable task even today. This is largely due to the complicated deformation behavior of the solder material under elevated temperature.

Finite Element Analysis (FEA) is the most commonly used tool to study the solder behavior under thermal loading. Many different FEA-based solder models exist in the literature. They differ primarily on the fundamental mechanism viewed as being responsible for inducing crack damage. Some of such models include strain-based, stress-based, energy-based, or the recently introduced damage model based on fracture mechanics. A review on all major solder fatigue models can be found in [1].

Among all solder-fatigue life models, the energy-based method is arguably the most popular one [2-12]. Over the years, the method has been applied to many types of packages. Excellent correlation with the actual test results was reported in [7]. The energy-based method links the fatigue life to the inelastic strain energy dissipation of solder joints. Based on extensive test of BGA solder joints and FE modeling, Darveaux proposed empirical equations to calculate the solder fatigue life [2-4]. In Darveaux's model, the total fatigue life consists of the life before crack initiation and the life after it. The constant terms are derived by curve-fitting the FEA prediction with the test data. Because the inelastic strain energy depends strongly on the finite element mesh of the solder joints, different constants values were given according to the element size. According to Darveaux, good correlation with the test data can be expected only when the solder joints are meshed such that the element size in the solder height direction has fixed values that fall in the range specified in [4].

In recent years, as the trend toward minimization continues to drive the electronic packaging industry, Wafer Level Chip Scale Package (WL-CSP) has emerged as an ideal solution for low to mid pin-count applications. The advantages of using WL-CSP over other packaging types include space savings and excellent electrical performance. One example of such packages is National Semiconductor's micro SMD, which is regarded as a true WL-CSP because it eliminates the substrate or interposer completely, and hence the silicon die itself is the package. Solder bumps are used to connect the die to the PCB.

Solder reliability is a critical issue for wafer level packages such as micro SMD. First, most of the micro SMD packages are used without underfill, which can improve solder reliability by relieving the solder stresses during thermal cycling [13]. Second, the thermal mismatch between the package and the PCB is more prominent than in the

similar-looking BGA packages, where the BT substrate, having similar Coefficient of Thermal Expansion (CTE) as the PCB, serves as a soft cushion to relieve such mismatch.

Previous works on solder reliability for WL-CSP are scarce but can be found in [8-10, 14-15]. In [15], a fracture mechanics-based approach was used to calculate the stress intensity factor assuming the existence of crack in the beginning of the process. In [8-10], Darveaux's model was re-applied to calculate the fatigue life of WL-CSP. However, none of the above literature provides a comprehensive evaluation on the accuracy of Darveaux's model for WL-CSP.

In addition to the lack of documented correlation with the test data, no literature appears to consider the effect of solder geometry on the fatigue life calculation. The solder bump used in micro SMD package has a much smaller geometrical scale than the typical BGA balls. Given this, it may become difficult or even impossible to maintain the appropriate element as recommended by Darveaux in [4]. When significant disparity arises in meshing the solder joints, using the same constants in [4] may yield unacceptable error in the fatigue life calculation. Unfortunately, to the best of the authors' knowledge, this aspect has been largely left undiscussed in the current literature.

To address the aforementioned limitations, we propose in this paper a new energy-based solder fatigue model for micro SMD packages. Part of the motivation was from an early study that used Darveaux's model, in which the large discrepancy between test data and simulation data was identified but left unaddressed [9]. The new model uses the same mathematical equation form to describe the crack growth rate, the constant terms used in the equation are acquired by correlating the fatigue life with tested values in a least-square minimization process. Unlike Darveaux's model, in which separate equations are used to describe both crack initiation and crack growth. The current approach assumes fixed ratio between lives associated with crack initiation and crack growth, hence reduces the total number of equations required from 2 to 1. Even with this simplification, the new model still achieved overall better accuracy than Darveaux's model.

National Semiconductor's micro SMD Packages

National Semiconductor's Wafer Level-Chip Scale Package (WL-CSP) is well known in the industry as the micro SMD [16]. The micro SMD, a true wafer scale package has proven to be highly adaptable in the conventional assembly process, requiring no special considerations during the surface mount assembly operation. The current micro SMD utilizes standard eutectic Sn/Pb as well as the option to have lead-free Sn/Ag/Cu solder bumps as the interconnect medium. There are two bump sizes currently available for the micro SMD package, a 170-micron bump diameter and a 300-micron bump diameter.

In WL-CSP, the die and package are processed and tested on the wafer, prior to singulation. The technology offers a number of advantages: lower cost with larger wafer size and/or smaller die size; more savings since packaging and test are carried out at the wafer level; simplification in

shipping and handling logistics; and compatibility with standard surface mount processes. As a result, wafer level packaging has seen wider use of late.

The predominant application of the micro SMD package has been seen in the mobile electronics applications like cellular phones, personal digital assistants, pagers, notebook PCs among others. The small size, low-cost, diverse functionalities available, and the ease of use make this a package of choice for portable electronics.

Solder Joint Reliability Evaluation

Typical reliability testing of micro SMD assemblies involves several types of accelerated stress testing like (but not limited to) thermal cycling, thermal shock, temperature-humidity-bias testing, autoclave test and operational/functional tests. As with most WL-CSP packages, most of these tests are carried out at the board level. This form of test is especially insightful in the case of thermal cycling and shock since the thermal mismatch between the components of the assembly (standard FR-4 test boards, solder joint, and silicon) are the basis of the stresses generated in the assembly.

Multiple profiles were used in thermal excursion testing. It involved shock testing (-40°C to +125°C with a time profile of 14-minute hold at extreme temperatures and 3-minute ramp; or -25°C to +125°C with a time profile of 9-minute hold at extreme temperatures and 1-minute ramp) as well as thermal cycling tests (-40°C to +125°C with a time profile of 15-minute hold at extreme temperature and 15-minute ramp). For thermal shock testing, the minimum passing requirement is 500 cycles without a single failure while thermal cycling test requires 750 cycles without a single failure.

The model generated attempts to address the thermal shock related thermal profiles used in the actual testing and simulate the same test conditions. Other conditions like package thickness and board thickness, which also play a significant role in board level reliability, were also included. During the testing involving thermal excursions, several board (FR-4) thickness ranging from 32 to 62 mil were used to gauge impact and assess credible performance for all possible assembly conditions.

Throughout the testing conducted, a failure was defined as failure in test for any of the device functionality criteria. These criteria include continuity failure of a joint, and/or any deviation from specified values in product specification such as shifts in output voltages, current, or power ratings.

Weibull plots for the failure data are generated using statistical tools. A Weibull plot is a presentation of the time to failure data on a logarithmic scale. These plots are used to generate the base model parameters by using the β (slope of plot) and η (estimated Weibull life) from the plots. In general, typical Weibull life plots for the various combinations show that Weibull life (time-to-failure for 63.2% of the sample size) goes on increasing as the bump count (and therein the die size) is reduced.

Failure analysis on the failed parts revealed that the failure mode consisted of cracks in the bulk solder joint close to the package-pad. This is a known failure mechanism, confirming

that the failures were caused by solder joint fatigue. A cross-section view of the solder cracks in micro SMD can be seen in *Figure 1*. Since the model attempts to predict the life of a solder joint and hence the assembly itself based on the crack initiation time and propagation rate, solder fatigue as the primary failure mode lends credence to the model's assumptions regarding the mode of failure.

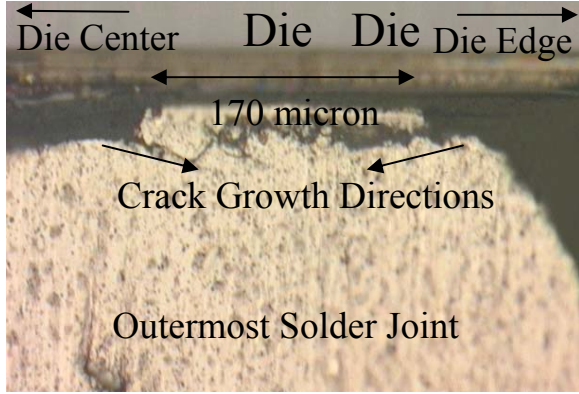


Figure 1: Typical examples of solder cracks in micro SMD package

Energy-based Method using Non-linear Finite Element Analysis

The energy-based method links the fatigue life to the inelastic strain energy dissipation of solder joints. Based on extensive test of BGA solder joints, Darveaux proposed the correlations to calculate the solder fatigue life [1-4]. In Darveaux's model, the total fatigue life consists of the life associated with crack initiation and the life associated with crack growth. The number of cycles before crack initiation N_0 was calculated as:

$$N_0 = C_1 \Delta W^{C_2} \quad (1)$$

where ΔW is the incremental inelastic energy per cycle at the stable cycle, and at the solder joint in concern, C_1 and C_2 are constants.

A similar form of equation was also derived to calculate the crack growth rate per cycle da/dN :

$$da/dN = C_3 \Delta W^{C_4} \quad (2)$$

again, C_3 and C_4 are two more constants that need to be determined by tests.

The total number of cycles before failure, N_a can thus be written as:

$$N_a = N_0 + \frac{a}{da/dN} \quad (3)$$

where a is the total distance the crack has to travel before failure, which is defined as the complete separation of solder joint from the package. For a solder joint, a can be conveniently interpreted as the solder diameter at the solder-die interface.

To alleviate the well-known mesh-dependence problem, Darveaux also made recommendations on the mesh size that should be used and different constants were calculated based on different mesh size. For the same reason, instead of using the absolute inelastic energy of the entire solder joint, a volume-averaged energy term, ΔW_{ave} was introduced and defined by:

$$\Delta W_{ave} = \frac{\sum_{i=1}^n dW_i V_i}{\sum_{i=1}^n V_i} \quad (4)$$

where dW_i is the incremental inelastic energy of element i at the first stable cycle, n is the total number of elements considered and V_i is the calculated volume of element i . It appears that different choices exist in the current literature on how to choose the control volume. However, all agree that the volume should always include the region on the joint where the highest stress is expected.

1-Step modeling vs. Global-local modeling

Full-scale FEA of solder joint under temperature cycling condition represents a challenging task primarily because of the highly non-linear deformation behavior of solder material at elevated temperature, and also because of the large number of solder balls that need to be modeled. When facing limited computer resources and short time, it is critical to make as much simplification in the model as possible, yet still capture the essential solder behavior. Motivated by the discussion in [11] and in [12], the alternative modeling approach we chose was to construct a global model and a local model. The global model contains a complete package attached to a PCB. However, the solder-die interface is simplified in order to reduce the model size. The local model, on the other hand, includes only one solder joint and part of the die and part of the board. All layers of material in the solder-die interface are faithfully captured in the local model. An interface is defined between the two models such that the nodal displacements calculated by the global model can be transferred to the local model as its boundary condition. The advantages of the 2-step model or global-local approach is that both models can be maintained sufficiently small in size, and therefore requires less computer run time. However, accuracy may suffer somewhat because of the simplification made in constructing the global model.

It should be noted that in [12], only one linear elastic analysis is carried out for the global model, subject to a 1°C temperature change, the displacement received due to such loading were then scaled back according to the temperature steps in the local model. Essentially, this assumes that all the materials have temperature-independent properties in the global model and therefore the displacement is linearly proportional to the temperature loading. Given the fact that solder retains only about half of its room temperature modulus at 120 °C, it was felt that making such assumption might jeopardize calculation accuracy. Hence, our global model incorporates temperature-dependent material properties.

ANSYS 7.0 was the finite element analysis tool in our study [18]. Both the global models and the local models were developed using parametric ANSYS scripts that allow the change of geometry and mesh density with ease. Overall, a total of more than 3000 lines of ANSYS scripts was written to create two models. ANSYS plots illustrating the 3-D view of the models are shown in *Figure 2*. Due to symmetry, only ¼ or ½ of the package/board was modeled in the global model, the worst-stressed solder joint was assumed to be the corner joint, and hence, ½ or 1 of the corner joint was modeled in the local model, depending on package symmetry. Because temperature dependent material properties were used on the global model, multiple cut-boundary operations were performed to transfer the loads between two models.

Material properties can be found from [8]. In particular, for the solder material, Anand’s constitutive model [17] was employed. The Anand’s constants were taken from [8]. For solders and FR-4 board, temperature-dependent material properties were defined.

The volume used to calculate the averaged energy is chosen as the layer of elements that is immediately below the neck section of the joint. The corresponding fatigue life was calculated according to Eqs. (1) – (3).

The $N_{(50\%)}$ or characteristic life was used as the metric to judge the modeling data. The $N_{(50\%)}$ can be easily acquired from Weibull plots. Using 1-step model and equation (1) to (3), we calculated $N_{(50\%)}$ life for 8, 10, 14, 16, 18, 25, 36, and 64 bump micro SMD packages and listed the results in *Table 1*. For comparison, the $N_{(50\%)}$ lives from the Weibull plots are given in the same Table and the percentage errors were shown. Similarly, *Table 2* contains the results when using global-local model.

Table 1: Package fatigue life and FEA prediction using 1-step model and Darveaux’s equations

Bump Count	Data Type	Fatigue Life	FEA Life	Percentage Error
8L	Test	1529	1452	5.0
10L	Test	1057	1227	16.1
14L	Test	880	953	8.3
16L	Test	809	974	20.4
18L	Test	920	1039	12.9
25L	Test	1132	1158	2.3
36L	Test	920	615	33.2
48L	Test	856	526	38.5
64L	Test	592	456	22.9

For the 1-step model, our data showed that the correlation error was between 2.3% to 38.5%, with maximum error corresponding to the 48 bump package. Furthermore, FEA lives agree well with the test data for low to mid pin count packages but tends to be very conservative for high pin count packages. The global-local model, on the other hand, underpredicted the fatigue life in all cases, especially when the pin-count is high. The error range was between 8.5% to 53.0%, which is poorer than the 1-step model. In summary,

for micro SMD packages, Darveaux’s model failed to achieve the same accuracy level as typically seen in PBGA packages.

Revised Formula for micro SMD Packages

The poor correlation accuracy of using Darveaux’s model may attribute to the strongly mesh-dependent inelastic dissipation calculation. The extent of this dependency was lessened by observing the rule Darveaux proposed to define the element thickness in the solder height direction. However, due to the drastic difference in size between WL-CSP balls and PBGA balls (for example, a typical PBGA ball

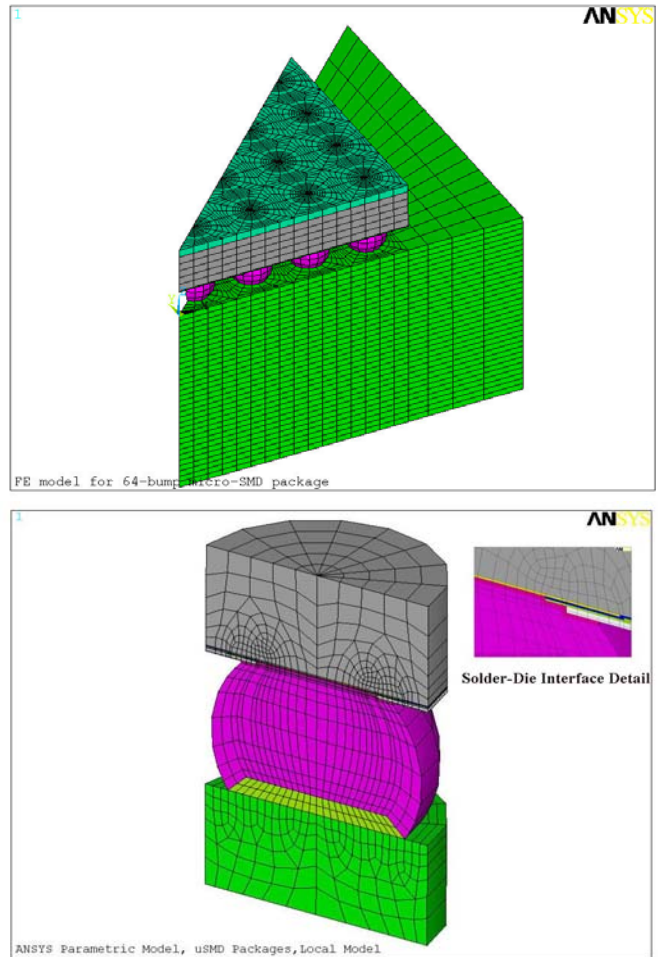


Figure 2: ANSYS plots illustrating the global model for a 64-bump micro SMD (Top) and the local model (Bottom). The 1-step model shares the same mesh as the global model. The inset shows details at solder-package interface.

has a diameter 3 times larger than a typical WL-CSP ball), the element in the radial direction of the solder ball may also have significant influence on the energy calculation.

To reduce this mesh-dependency to its minimum, it is necessary to regenerate all the constant terms defined in Equations (1) and (2). This implies repeating the same curve-fitting process Darveaux had gone through in [1], but using the new test data for micro SMD. One difficulty arose in curve fitting the crack initiation life due to the lack of test data. To overcome this, we assume that a fixed ratio exists between crack initiation life and crack growth life, and hence

Table 2: Package fatigue life and FEA prediction using global-local model and Darveaux's equations

Bump Count	Data Type	Fatigue Life	FEA Life	Percentage Error
8L	Test	1529	1087	28.9
10L	Test	1057	931	11.9
14L	Test	880	727	17.4
16L	Test	809	740	8.5
18L	Test	920	791	14.0
25L	Test	1132	871	23.0
36L	Test	920	468	49.1
48L	Test	856	402	53.0
64L	Test	592	350	40.9

Table 3: Package fatigue life and FEA prediction using 1-step model and equation (7)

Bump Count	Data Type	Fatigue Life	FEA Life	Percentage Error
8L	Training	1529	1101	28.0
10L	Training	1057	1121	6.0
14L	Training	880	971	10.3
16L	Training	809	933	15.3
18L	Training	920	1047	13.8
25L	Training	1132	1072	5.3
36L	Training	920	789	14.3
48L	Test	856	745	12.9
64L	Test	592	708	19.6

Table 4: Package fatigue life and FEA prediction using global-local model and equation (7)

Bump Count	Data Type	Fatigue Life	FEA Life	Percentage Error
8L	Training	1529	1100	28.1
10L	Training	1057	707	33.1
14L	Training	880	667	24.2
16L	Training	809	639	21.0
18L	Training	920	715	22.3
25L	Training	1132	880	22.3
36L	Training	920	699	24.0
48L	Test	856	672	21.4
64L	Test	592	644	8.9

both processes can be described by Equation (2), with a constant added for the crack initiation life. The following equation defines the new model:

$$N_a = N_0 + \frac{a}{da/dN} = (C_0 + 1) \frac{a}{da/dN} = (C_0 + 1) \frac{a}{C_3 \Delta W^{c_4}} \quad (5)$$

Rearranging the constant terms, Equation (5) can be written as:

$$N_a = \frac{a}{C_3 \Delta W^{c_4}} \quad (6)$$

where:

$$C_3' = \frac{C_3}{C_0 + 1}$$

For area array packages, based on our experience, the crack initiation period is usually brief while the crack growth takes much longer time. In other words, C_0 is close to zero. Therefore, even though some variation exists in C_0 for different packages within micro SMD, it is still reasonable to assume that C_3 approximately remains as a constant.

To calculate C_3' and C_4 is to match Equation (6) with the test data. Mathematically, this process can be described by minimizing the following error function f , defined as the 2-norm error between test data and the FEA prediction:

$$\min. f(c_3', c_4) = \sum_{i=1}^M \left(N_i - \frac{a}{c_3' \Delta W_i^{c_4}} \right)^2 \quad (7)$$

where N_i is $N_{(50\%)}$ from test for package i and M is the total number of packages included.

Equation (7) was first solved using both the 1-step model data and global-local model data. The 8, 10, 14, 16, 18, 25, and 36-bump micro SMD were included when solving for C_3' and C_4 . The new formula was then used to predict the fatigue life for 48 bump and 64 bump package, to which the tested $N_{(50\%)}$ are also known. Complete results, including calculated fatigue lives for packages that are used to solve Equation (7), can be found in *Tables (3) and (4)*.

Discussion

As expected, overall, the new formula achieved better accuracy compared with Darveaux's model. In particular, for 48 bump and 64 bump packages, both 1-step model and global-local model were able to achieve an accuracy level that is roughly within 20% of the test data, which is very encouraging since Darveaux predicted the correlation error to be within 25% for such finite element-based model.

Overall, the equation based on 1-step model has shown better fit to the test data than the global-local model, this is primarily due to the exclusion of solder creep in the global model. In terms of efficiency, the global-local model was found to be superior, especially for high pin-count packages. Please refer to *Table 5* for computer time comparison.

The correlation error may be attributed to the following:

1. Package geometry tolerance due to manufacturing variations that can not be incorporated into the finite element model.
2. Inaccurate material behavior representation, for example, only properties at room temperature are available for the back-coating material, while in reality the material may exhibit strong temperature dependency. Also, the material properties of the PCB used in the test were taken from a standard reference, which may be different than the actual PCB used.
3. The assumption that the ratio between crack initiation life and crack growth life is a constant may be valid only as a first order of approximation. A separate formula for the crack initiation life may improve the accuracy.

Table 5: Computer run time (in hours) using local-global model or 1-step model. A SUN workstation (Sunblade 2000 with 900Mhz clock speed and 2Gb RAM) was used for all calculation

Bump Count	Local-Global	1-Step Model
8L	1.3	2.3
10L	4.7	10.0
14L	4.0	4.2
16L	1.7	2.4
18L	7.3	4.3
25L	2.7	3.5
36L	3.6	9.6
48L	5.8	27.2
64L	4.0	18.6

Conclusions

In this paper we proposed a new empirical equation to calculate the package fatigue life for WL-CSP. The new equation is based on calculating the inelastic energy dissipation of the solder joint and shares a similar mathematical form as the one proposed by Darveaux in [1]. It was found that Darveaux's model did not capture the fatigue life for WL-CSP well, and hence the current study. To simplify the curve-fitting process, we assume that a fixed ratio exists between the crack initiation life and crack growth life, therefore, only one equation is needed to predict the total fatigue life of the package. The constant terms used in the equation were calculated by curve-fitting the simulation data with test results in a least square minimization process. Overall, the new equation performed better in accuracy and was able to achieve within 20% correlation error in life prediction. This is comparable to what Darveaux's model achieved for PBGA packages.

In addition, the impact of different modeling schemes was also evaluated in terms of their accuracy and efficiency. Two choices considered included a single global model and a global-local model. In terms of accuracy, the single global model was found to be superior to the global-local model. However, it was more demanding in computer resources, and generally was associated with longer run times.

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