Reliability of Chip Scale Packages under Mechanical Shock Loading

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Abstract

The reliability of different chip scale packages (CSPs) were studied under mechanical shock loading. The tests were carried out according to the JESD22-B111 standard. An area array with 100-bumps and pre-applied underfill, an area array with 36-bumps (no underfill), and leadless leadframe packages (LLP) with 8- and 48-leads were employed. In addition, the impact of three different printed wiring board (PWB) protective coatings was investigated: Ni(P)|Au, organic soldering preservative (OSP), and Ag on the copper soldering pads.

It was found that the smaller package sizes yielded better reliability results than the larger components. In addition, interconnections on Cu|OSP were the most reliable, whereas those on Ag were the least reliable. It is proposed that the dissolved Ag strengthened the solder interconnections, and thus affected the stress levels under mechanical shock loading conditions. The failure modes were different from those commonly observed in drop tested component boards. In this work, the failure mode was cracking of the copper traces leading out of the solder interconnections, and the mode was the same regardless of the component type. The different interconnection geometry and rigidity of the components evoked stress concentrations in the PWB around the components, and thus made the cracks propagate through the copper line of the board instead of the solder interconnections. Furthermore, it was also found out that the die attach interconnection (DAI) underneath the component stiffened the structure and increased stresses in the PWB around the edges of the components. When the die attachment was not soldered, the drops-to-failure doubled with the components having Sn terminal finish, but the failure mode changed as well.

Keywords: Drop test, WL-CSP, LLP, JEDEC, reliability, PWB metal finish, Weibull, failure mode and mechanism.

Introduction

Electronics manufacturers have been successful in making ever smaller and lighter weight portable products equipped with an increasing number of functions. This development has been facilitated by the adoption of chip scale packages (CSP), which are a reasonably low-cost solution for the production of small scale, high density portable products. However, increasing interconnection densities and decreasing interconnection volumes create considerable reliability challenges. Because the finer pitch components are placed closer to the printed wiring boards (PWB), solder interconnections experience considerably increased strains and stresses. Furthermore, the adoption of new lead-free materials gives rise to reliability concerns due to the growing complexity of solder metallurgies. New combinations of solder pastes, PWB protective coatings, and component terminal metallizations produce unforeseen microstructures and defects in increasingly smaller solder interconnections.

Portable electronic products are especially prone to fail due to mechanical shock loads caused by dropping. These loadings are simulated with standardized reliability tests [1] that also allow comparative studies of different material combinations. Because different material combinations have different lifetimes under certain loading, the reliability must be studied systematically by involving both physics-of-failure and statistical approaches. Statistical methods are needed for study of the failure rates and to classify the failure modes, as well as to make inferences regarding differences between lifetimes under tests.

Recent studies on the drop test reliability of chip scale packaged ball grid arrays (BGA) have shown that the intermetallic layers between solder and contact metallizations are likely to fail in the drop test [2-8]. Cracks typically nucleate at the corners of the interconnections, a safe distance away from the intermetallic compound (IMC) layers in the bulk solder, but jump very quickly into the IMC layers, which obviously provide a favorable path for cracks to propagate due to the brittle nature of the compounds [2]. The failure modes and the failure mechanism of drop tested assemblies are very different from those observed after thermal cycling. This is because the plastic behavior of the solder is strongly strain rate-dependent at room temperature (~295K), which is relatively high ($0.6T_m$) as compared to the melting point of the solder (~500K). Solders become remarkably stronger as the strain rate increases from that occurring in thermal cyclic tests to that occurring in drop tests [3,9]. Thus, due to the strain rate hardening of the solder interconnections, the stresses become much higher and more concentrated in the corner regions of the interconnections, where they exceed the fracture strength of the weakest reaction layer. In thermal cycling, where the strain rates are relatively low, the interconnections fail by recrystallization-induced fatigue fracture, where the cracks nucleate and grow along the grain boundaries of the recrystallized grains.

Failure modes and mechanisms controlling the reliability of different wafer level-chip scale packages (WL-CSP) and leadless leadframe packages (LLP) as well as the effect of PWB surface finish under shock loading conditions was investigated in this paper. The reliability was studied by employing a large number of test structures and by investigating statistically the differences between times-to-failure. Detailed fractographic and microstructural studies was carried out in order to have a better understanding of the failure modes and mechanisms in operation. In addition to experimental tests, the behavior of the assemblies during the drop testing and the stresses generated in the solder interconnection was analyzed with the help of finite element method (FEM).

Materials and Methods

The following components were used: leadless leadframe package (LLP) with 8- or 48-leads, and an area array (AA) CSP with 36- or 100-bumps. The 8-L is similar to the widely used industry configuration of Dual Flat No-Lead (DFN). The 48-L is equivalent to the industry Quad Flat No-Lead (QFN). The LLPs had a relatively large die attach pad (DAP) underneath the components, which is soldered onto the PWB in order to provide good heat conductivity from the component. The AA100 package had pre-applied underfill while no underfill of any kind was used with the AA36. Component dimensions and under bump metallurgies (UBM) are presented in *Table I* and the component layouts in *Figure 1*.

The high-density circuit boards (1+6+1 build-up FR4) were manufactured by the Aspocomp Group with three different protective coating options on the Cu soldering pads: about 2 μm thick Ni(P)|Au [Ni: 2 μm, Au: ~0.02 μm, 9 wt-% P in Ni], 0.2-0.5 μm thick organic solderability preservative (OSP), and 0.5-0.7 μm thick chemical Ag. The test board was designed according to the JESD22-B111 board level drop test standard (see *Figure 2*) [1].

The circuit boards were assembled using Sn3.8Ag0.7Cu (Multicore) solder paste. The solder paste was printed (DEK 265 Horizon) with a 127 mm thick laser drilled stainless steel stencil and metal squeegees. The mounting machine (Philips ACM Micro) was set to achieve the highest possible accuracy ($\mu+5\sigma < 30$ μm, $C_{pk} = 1.67$), and the reflow was carried out in a conventional forced convection oven (EPM/Heraeus EWOS 5.1 N2) under air atmosphere. The temperature profile was set according to the recommendations of the solder paste manufacturer. The peak temperature underneath the components was measured with a profilometer (ECD Super M.O.L.E. Gold) as 246±0.5ºC, and the time above 217ºC was 45±1 seconds depending on the component location.

After the post-reflow inspection the assemblies were drop tested according to the JESD22-B111 standard. Condition B of the standard was used (peak deceleration of 1500 G and pulse width of 0.5 ms). Deceleration was measured (National Instruments PXI-4472) from the board attach fixture. The event detector (Analysis Tech 128/256 STD) was connected to the test boards by soldering. A failure was recorded when the resistance through the daisy chain network exceeded the 1 kΩ threshold resistance for 200 nanoseconds four times in a sequence of six drops. All electrical connections were checked before interpreting the increase as a failure.

The failure modes were studied from cross-sections prepared by standard metallographic methods. Cross sections

Table I: *Component specifications.*

Package Type	Package Dimensions	Pad Size / Bump Size	Pitch	UBM
LLP8	2.5 mm x 2.5 mm x 0.8 mm	0.25 mm x 0.6 mm	0.5 mm	Ni|Pd|Au or Sn
LLP48	7.0 mm x 7.0 mm x 0.8 mm	0.25 mm x 0.6 mm	0.5 mm	Ni|Pd|Au or Sn
AA100	5.0 mm x 5.0 mm x 0.7 mm	0.3 mm (diameter) 0.25 mm (height)	0.5 mm	Ni(V)|Cu
AA 36	2.5mm x 2.5 mm x 0.6 mm	0.25 mm (diameter) 0.2 mm (height)	0.4 mm	Ni(V)|Cu

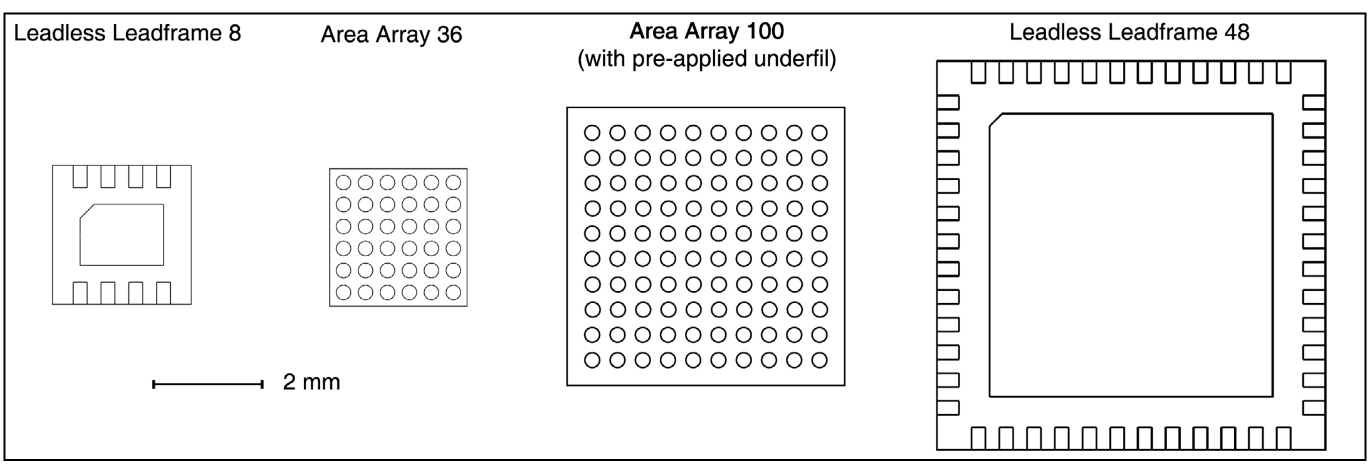

Figure 1: *Layouts of the components used in this work.*

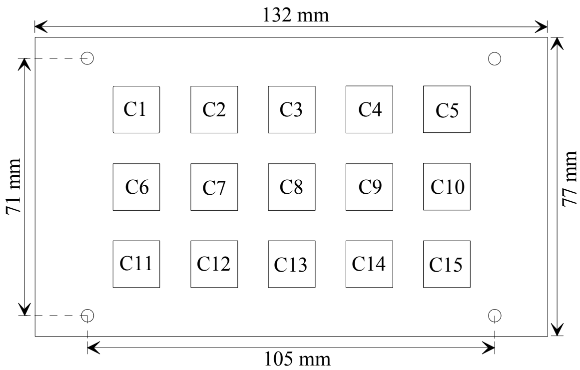

***Figure 2**: Component layout of the JESD22-B111 compliant test board.*

were investigated with optical (Olympus BX60) and scanning electron (JEOL 6335F) microscopes.

The difference in reliability performance is evaluated on the basis of average drops-to-failure. Parametric methods require the assumption that the data is normally distributed. The Shapiro-Wilk Test, for instance, can be used to study the conformance of the data to the normal distribution [10]. When the drops-to-failure does not follow the normal distribution, nonparametric methods, such as the Wilcoxon Rank-Sum Test, must be used to test the equality of two populations [10]. Conclusion in this paper are made at less that 5% risk level (α), which means that if the resulting p–value of the test is below 5 %, there is a good reason to reject the null hypothesis.

The reliability of the solder interconnections was studied by making use of the statistical Weibull reliability analysis. The three-parameter cumulative Weibull distribution function is given by:

$$F(t) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right],$$

where F(t) is the cumulative density function, η is the characteristic lifetime, β is the shape parameter, and γ is the failure-free lifetime. If the failure data plot with a concave trend and the fit of the regression is therefore poor, it may indicate a presence of a failure-free lifetime, and the third parameter γ is introduced. Otherwise, the γ equals zero.

The effect of the die attach interconnection (DAI) between the LLP48 component and the PWB on stresses in the solder interconnections around the component was analyzed by employing the finite element method (FEM). Two models were constructed for the calculations: one with the die attachment pad soldered to the PWB, and one without soldering the pads. Calculations were carried out with ABAQUS by using axisymmetric models of the component and the piece of PWB that was 20 mm in diameter. Boundary conditions were such that at the centre of the model, the horizontal displacements of the component were fixed as well as the horizontal and vertical displacements of the board. The models were loaded by applying 2 mm vertical displacement downwards at the perimeter of the board. Only elastic material properties were used due to high deformation rates in drop tests and the related strain rate hardening of solder [2].

Results and Discussion

The reliability test procedure was constructed as a full factorial design with six replications. The type of component and PWB coating were the main variables. In order to make use of as many data points as possible in statistical analyses, the locations where the components experience nearly equal mechanical loadings were determined on the basis of the drops-to-failure, strain measurements, and finite element calculations. Two symmetrically located components, components C3 and C13 in *Figure 2*, were pooled and thus 12 data points per material combination were used in the numerical analyses. The results from the drop tests are presented in *Table II* with averages of the different variable combinations.

The LLP components had two different terminal finishes (Ni|Pd|Au and matte Sn) and their effect on the reliability was studied first. The Shapiro-Wilk Test for normality showed that the test data did not conform to normal distribution and therefore the non-parametric Wilcoxon Rank-Sum Test was used to carry out the significance testing. The results show that with the LLP8, the matte Sn finish on the component side yields higher drop test reliability than the Ni|Pd|Au (α < 0.1 %). In the case of LLP48, however, the effect of the component terminal finish fails to be significant.

The effect of the PWB protective coating on the drop test reliability was studied in the same manner: interconnections

***Table II**: Average drop-to-failure of the different variable combinations.*

Average drops-to-failure	LLP8		LLP48		AA100	AA36	
	Ni|Pd|Au	Sn	Ni|Pd|Au	Sn	Ni(V)|Cu	Ni(V)|Cu	Average
Ni(P)|Au	13	29	10	6	56	119	23
OSP	20	32	14	17	63	237	29
Ag	9	21	7	7	39	83	17
Average	14	28	10	10	53	146	19

***Table III**: Weibull parameters: characteristic life (η), shape parameter (β) ± 95% confidence interval, and location parameter (γ).*

Weibull η / β±95%c.i. / γ	LLP8		LLP48		AA100	AA36
	Ni|Pd|Au	Sn	Ni|Pd|Au	Sn	Ni(V)|Cu	Ni(V)|Cu
Ni(P)|Au	6 / 1,1 ± 0,2 / 7	19 / 1,2 ± 0,2 / 12	10 / 8,0 ± 2,8 / 10	7 / 4,2 ± 0,7 / 0	41 / 2,6 ± 0,3 / 20	50 / 1,5 ± 0,1 / 75
OSP	10 / 2,5 ± 0,6 / 12	8 / 1,1 ± 0,2 / 25	5 / 1,4 ± 0,4 / 15	18 / 7,2 ± 1,3 / 0	44 / 2,8 ± 0,3 / 24	76 / 1,7 ± 0,2 / 109
Ag	9 / 4,3 ± 0,8 / 0	6 / 1,6 ± 0,2 / 16	4 / 3,4 ± 1,1 / 8	6 / 7,5 ± 1,1 / 0	22 / 2,2 ± 0,4 / 20	36 / 1,1 ± 0,1 / 49

soldered on the OSP-coated soldering pads are more reliable than those soldered on the Ni(P)|Au (α < 0.1 %) and interconnections on Ag-coated pads are the weakest (α = 3.2 %).

The drops-to-failure of different components was studied next. The component AA36 is more reliable than the AA100 (α < 0.1 %), the AA100 is more reliable than the LLP8 with Sn finish (α < 0.1 %), the LLP8 with Ni|Pd|Au finish is more reliable than either of the LLP48s (α = 1.4 %), and there is no statistically significant difference between the LLP48s with different finishes (α = 19.5 %). The different Weibull parameters of each variable combination are presented in *Table III*.

The failure analyses revealed that the electrical breakdown of the components' daisy-chain structures was caused by cracking of the copper traces at the edge of the interconnections on the PWB (see *Figure 3*). The failure mode was the same regardless of the component type. Failures of copper wires have been observed also elsewhere [11].

This is a different failure mode from what has previously been observed in the drop testing where cracks propagated along the intermetallic layers on either side of the interconnections [2-5]. The most significant difference as compared to the studies carried out earlier is the size and structure of the components. The component used earlier was a 12 mm x 12 mm CSP-sized BGA with 80 µm thick flexible polyimide interposer. The number of bumps was 144 (500 µm diameter, 480 µm height, and 800 µm pitch) and the weight of the component was 0.3 g. If the interconnections on the LLP assemblies are compared to the one studied earlier, the interconnections are wider. This leads to different contact angle between solder and copper trace. In addition to the changes in the interconnection geometry, the underfill in AA100s and the die attach interconnection (DAI) in LLPs further changes the stress distribution in interconnections.

The stress distribution around the solder interconnections of the LLP48 was evaluated with the help of FEM in order to shed insight into the failure mechanism. The calculations (see *Figure 4 (a)*) show that stresses concentrate in the vicinity of the meniscus of the solder interconnections where the copper trace exits the interconnections.

The shape of the LLP interconnections is such that it increases the effect of copper wires on the reliability. The interconnections are long and wide when compared to their height making them more rigid than the barrel-shaped interconnections. The DAI structure further increases the rigidity of the structure by preventing the flexure of the PWB and, hence, increases stresses in the copper conductors. In order to find out the effect of the die attachment interconnection on the drop reliability, additional test boards (again 6 of each combination) were assembled without soldering the DAI and using the same processing parameters and methods of testing as with the earlier samples.

The results showed that the drops-to-failure increased (α < 0.1 %) with the components having Sn terminal finish while the drops-to-failure decreased (α = 1.3 %) with the components having the Ni|Pd|Au finish when the die attach

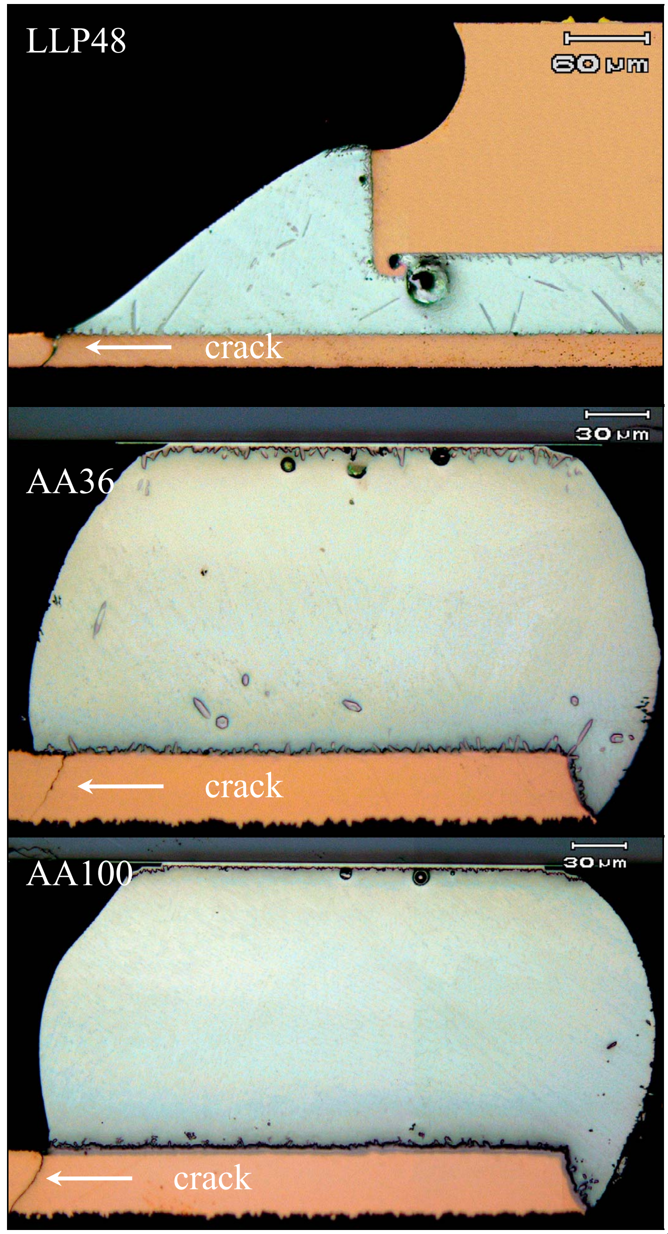

Figure 3: *Failure modes in the different types of components.*

PWB Coating	LLP48 with DAI		LLP48 no DAI	
	Ni|Pd|Au	Sn	Ni|Pd|Au	Sn
Ni(P)|Au	10	6	8	11
Cu|OSP	14	17		33
Average	12	12	8	22

pad was not soldered (see *Table IV*). The failure mode was a mixed mode of intermetallic fracture and cracking of the copper trace (see *Figure 5*). According to the FE analysis, the 5 mm x 5 mm DAP solder increases the maximum tensile stress in copper traces by 28 % when compared to the case where no solder is used (see *Figures 4 (a)* and *(b)*).

It should be noted that due to the very fast deformation rate, strength of solder interconnections is considerably increased and plastic deformation is subsequently reduced. The fact that plastic deformation occurring by dislocation slip

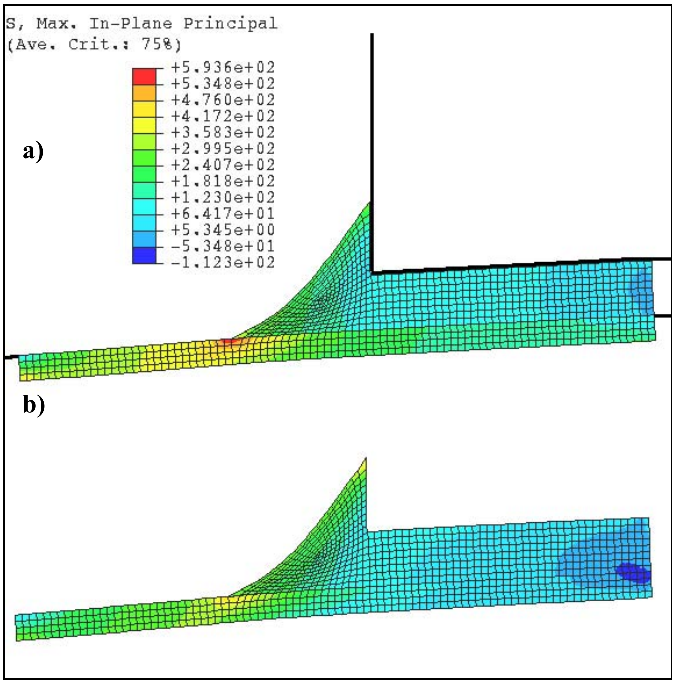

***Figure 4**: Maximum tensile stress (MPa) (a) with DAI soldered and (b) without soldering the DAI.*

is limited under shock loading conditions is evidenced by the presence of numerous deformation twins [3,4]. It is well known that alloying elements affect the reliability performance of tin-based solder interconnections by i) solid solution strengthening, and ii) dispersion strengthening.

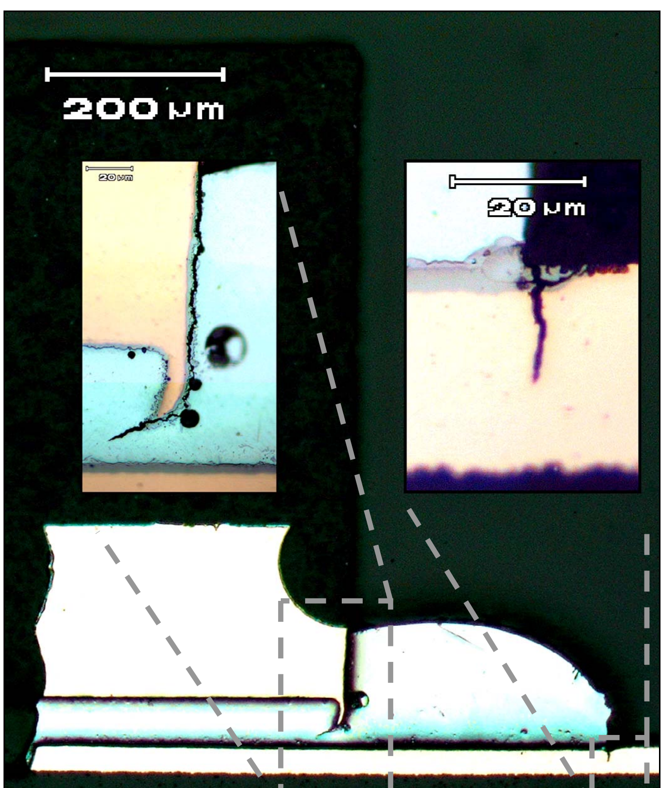

***Figure 5**: Mixed mode of intermetallic and copper trace fracture when the die attach pad is not soldered.*

Therefore, the strength of solder interconnections is affected by dissolving PWB protective coatings. The nominal composition of the solder interconnections in assemblies with Ag PWB surface finish was estimated from the metal contents of the solder pastes, the flux densities, the nominal compositions of the solder pastes, and the thickness of the Ag layer (~ 0.5 mm) on the soldering pads. The solder volume having the nominal composition of Sn3.8Ag0.7Cu is further alloyed by Ag to Sn4.8Ag0.7Cu due to the dissolution of the coating metal. It has been found out earlier that the shear strength of Sn3.5Ag (wt-%) solder increases considerably (dozens of percents) when the composition of solder changes to Sn5.0Ag (wt-%) [12]. This is expected to be the reason why the assemblies with Ag PWB protective coating were inferior to the Ni(P)|Au and Cu|OSP protective coatings.

Conclusions

Reliabilities of four different chip scale packages were studied under mechanical shock loading according to the JESD22-B111 standard. The impact of three different PWB protective coatings were also investigated: Ni(P)|Au, OSP, and immersion Ag.

Statistically significant differences in drops-to-failure were observed between the different CSP components as well as the protective coatings. From this perspective, the area array (WL-CSP) components were more reliable that the leadless leadframe packaged (LLP) components, and packages with smaller dimensions were more reliable than their larger counterparts. It could also be argued, however, that the joints of the LLP configurations are significantly stronger due to the large soldered die attach pad that fracture shifted from the joints to the next weakest link in the structure, namely, the thin Cu traces on the PWB. The failure mode in all cases was cracking of the copper traces leading out of these solder interconnections.

Furthermore, interconnections on Cu|OSP-coated PWBs were the most reliable, whereas those on Ag-coated PWBs were the least reliable. It was proposed that the dissolved Ag strengthens the solder interconnections, and thus increases the stress levels under mechanical shock load conditions. Furthermore, it was found out that the die attach structure underneath the LLP component stiffens the structure and increases stresses at the edges of the components. When the die attachment was not soldered, stresses decreased and the drops to failure increased with the components having Sn terminal finish. Also the failure mode changed to mixed mode of intermetallic and copper trace fracture.

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