Flexural Testing of Board Mounted Wafer Level Packages for Handheld Devices

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Abstract

With the growing proliferation of Wafer-Level-Chip-Scale-Packages (WLCSP), the target applications are increasingly focused on hand-held devices and consumer applications like cellular phones, pagers, PDA's etc. Packages in this family, like National Semiconductor's micro SMD package, have proven reliability in thermal cycling, humidity and bias testing, and are generally rated at moisture sensitivity level 1 (MSL-1). As applications continue to require more functionality in smaller packages, these package types will continue the growing trend of prevalence in the market-place.

Typical handheld applications like the cellular phone applications result in several cycles of flexing during normal application. Some cellular handset manufacturers have started investigating the need to implement a 'Push Button Test' to simulate the effects of repeated deflection of the PCB immediately under the keypads. This paper describes and discusses the results of extensive flexural testing done to understand the effect of flexural testing on wafer level components mounted on a PCB. The PCB configuration used attempted to approximate the PCB configuration typically seen with cellular phone applications. Multiple locations of component placement were selected with reference to the point of maximum flexing as well as distance to the nearest rivet/bolt location. Other parameters varied included the PCB build-up structure, and the landing pad sizes on the PCB at the soldering locations.

These experiments have shown a clear trend in terms of the superior solder joint strength achieved with an optimized solder joint shape, the importance of device location on the PCB to enhance life in flexural testing, and the impact of the overall size of the solder joint subjected to flexural testing. For all possible variations listed, based on a combination of the solder ball size, the correct pad size, and the location on PCB, there are positions on the PCB available which will surpass required test values. In case of limitations on some parameters, there is still a combination using the other factors that can create a solder joint strength that is able to withstand all requirements during flexural testing.

Introduction

The growth of wafer level packages has largely been driven by the requirements of portable electronics, predominated by applications like cellular phones and PDA's. These applications are human-interaction intensive; that is, a very large portion of the applications involve a manual input of a tactile manner. This introduces a variable element into the operation of these devices, since the manual input will vary in magnitude and time depending on the user.

Besides the typical reliability and life-cycle tests traditionally carried out for electronic packages, which include mechanical tests like drop tests and bending tests, the additional requirement from these packages includes flexural testing. As the Printed Circuit Boards (PCB) used become thinner together with the application profile, entire assemblies on PCB are subjected to flexing during application. This causes mechanical fatigue of the solder joints in package assemblies on the PCB. Failures caused by continuous or repetitive flexing depend on the location of the component location with respect to point of maximum flexure, proximity of the nearest rivet or bolt locations, PCB type and thickness, and the PCB pad configuration among other things. Prior work done has attempted to configure the test set-up to make it more standardized and more theoretically predictable. However, the actual application set-ups typically seen are more complex and result in stress patterns in solder joints that are significantly different from these standardized set-ups. An attempt to understand these various effects was made using micro SMD package devices from National Semiconductor's wafer level CSP package family.

Application Specific Information

Handheld applications are on a continued path of reduction in size. The lower the thickness of a handheld device, the better its ability to sell. Some of the latest offerings from leading manufacturers of cellular phones have clearly used their low thickness a major part of their marketing campaigns. With a very thin profile, the major focus is to make the contents as thin as possible. This includes the passive components, semiconductor IC's as well as the PCB itself. With the keypad itself also reduced to being an extremely thin membrane mounted on one side of the PCB, the pressure from the user's finger is directly transmitted to the PCB, with little or no buffer. Under such conditions, a relatively unbalanced, random-frequency force is placed on the PCB at varying locations, leading to deflections at those locations.

To truly model this variability, the goal of this effort was to have components mounted at varying distances from the point of force application. These locations would also have fixed distances from the mounting bolts or attachments. Hence each component location on the PCB would have a unique response to the application of a repetitive force to the PCB. Each component was monitored individually to measure this response. The result was to determine the best locations to place components, particularly the wafer level CSP packages on a given PCB layout.

Board Layout and Design

A four layer, double-sided PCB was used for this testing. The PCB dimensions were 5mm by 7.5mm and 1.0mm thick. These dimensions are representative of the typical PCB sizes seen in cellular handset applications.

Each PCB had thirty-one test sites on each side. Each site was designed to accommodate one daisy chain device

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with 8 solder bumps. This PCB design allowed characterization of the effects of component location on the number of cycles to failure noted in flexural testing. All pads on the PCB were non-solder-mask-defined and had an electroless-Nickel-immersion-Gold pad finish (ENIG). Two types of PCB build-up were used for the PCB: 1) FR-4 and, 2) Resin-coated-copper (RCC).

Two variants of the 8-bump micro SMD wafer level CSP were used. One had a 0.17mm bump diameter and the other had a 0.3mm bump diameter. Both devices used standard Tin-Lead (63/37) solder bumps.

One side of the PCB had 0.17mm pads, while the other had 0.3mm pads. On a given PCB, only one side was populated with the micro SMD devices for testing. With the options thus available it was possible to test various combinations of bump size with PCB pad size.

For the 0.17mm bump size micro SMD assemblies on the PCB, the stencil apertures were 0.3x0.3mm square with a 0.125mm thick stencil. For the 0.3mm bump size micro SMD, the stencil apertures were 0.25x0.25mm square with a 0.125mm stencil thickness. For all test assemblies, standard eutectic Tin-lead solder paste of the no-clean type was used for assembly.

Figure 1 shows the individual sites for mounting devices on the PCB. The figure shows the daisy chain network on the die as well as the continuation of the network on the PCB traces as well. Figure 2 shows a larger view of the overall PCB itself.

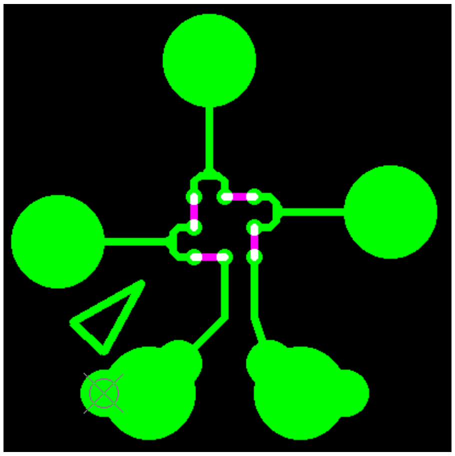

Figure 1: Individual test site for mounting WLCSP device

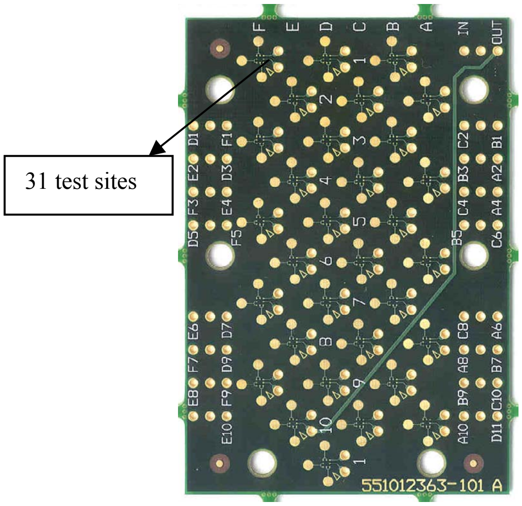

Figure 2: Overview of PCB

Test Equipment Set-Up

Repetitive cyclic deflection of the PCB was used as the external parameter to induce solder joint failure.

The key parameter measured was the number of cycles of deflection elapsed before any solder joint in the assembly failed. Failure was defined as an increase in network resistance by more than 50% for the particular device.

There are two ways to specify the bending parameter, deflection or force. For this characterization, flexural testing involved the cyclic bending of the Printed Circuit Board (PCB) with repetitive deflections that stressed the solder joints. The PCB was allowed to return to its rest position after every deflection. Figure 3 illustrates the test set-up used. In this figure the punch head or plunger is shown directly on the opposite side of a mounted device. However, other devices on the PCB are not necessarily under the plunger location at all times, and in fact have varying distances from the point of contact of the plunger to the PCB.

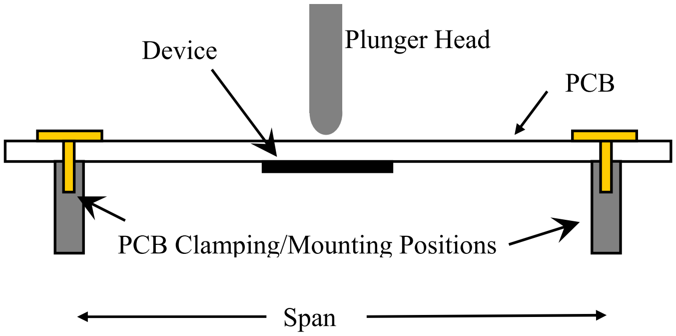

Figure 3: Illustration of test set-up, showing condition when plunger is directly behind the device location

An Instron tester (DynaMight 8841) was used for the repetitive flexural testing. The function of the Instron tester was providing the mechanical deflection, monitoring the output from the test boards, and displaying the number of test cycles at any given time.

Typically, the set-up used in off-the-shelf applications involves monitoring only a single output from the test board. In this case, since the desired application involved monitoring multiple locations on the test board simultaneously, an Altera UP2 Board (FPGA development board to implement digital logic) was used to monitor the output from the test board. This programmable board can monitor all outputs from the test board simultaneously. It can also pin-point the failed device and store the cycles at time of failure along with the device location in memory. An LED display provides a visual alert that also shows the failed location/device on the test board. In addition, an interface board was used that would provide feedback to the Instron tester to start or stop the test in case of failure noted by the Altera board.

The test procedure involved in this testing employed a ‘Stop Test’ instruction as soon as a failure was noted. Manual verification of the memory record and physical Instron record was made before providing input to restart the test after electrically providing a ‘jumper’ across the failed unit.

Figure 4 is a schematic showing part of the test set-up with six devices. The interface board has switches as shown that can be used to ‘jumper’ the network across any failed device location. The output from the Altera board is given back to the Instron to restart after a failure is noted and the interface board has triggered the affected switch.

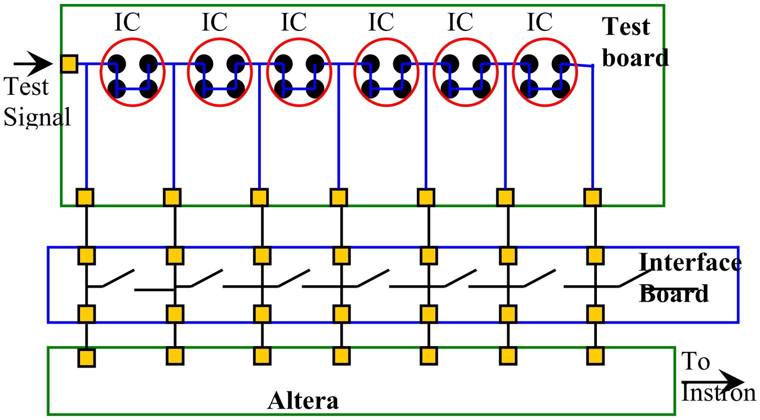

Figure 4: Test set-up schematic

The Instron tester with a test board mounted is shown in Figure 5. The plunger is shown in a ‘rest’ position above the test PCB. The components are on the bottom side of the PCB. Wires connected to the PCB transmit signals to and from the interface board.

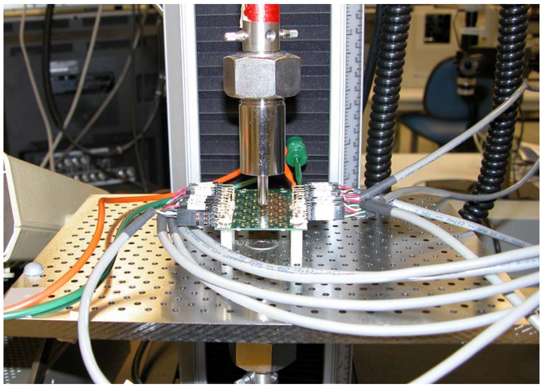

Figure 5: Instron tester with test board mounted

A schematic of the test board is shown in Figure 6 which indicates the individual device locations numerically. The ‘X’ mark indicates location where the plunger contacts the PCB repetitively. Two different maximum deflection values were used, namely 1.5mm and 2 mm. Prior works has suggested that results from deflections less than 1mm may be difficult to characterize repeat-ably. It needs to be understood by the reader that the maximum deflections used as part of this characterization are an accelerated way to induce failures, since in practice the maximum PCB deflections will be much lower.

A voltage of 5VDC was applied to the input, and the output was monitored. Criteria for failure was a 50% (or higher) increase in resistance measured at a given instant. In some cases, solder joints connect again when the deflection is removed, hence the need for instantaneous monitoring of output.

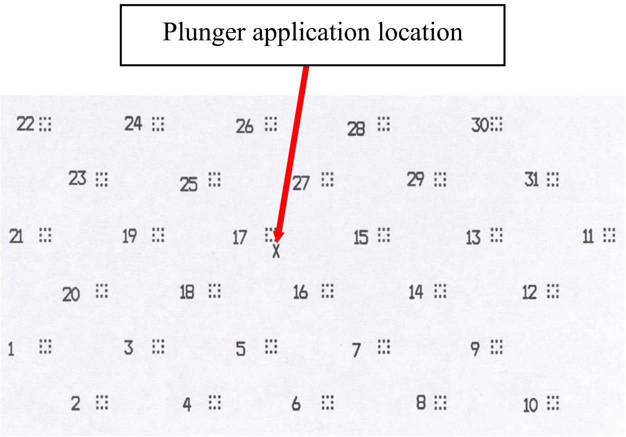

Figure 6: Schematic showing individual device locations on the test PCB

Each device location on the test board was assigned a number. The interface card monitored each location based on the number assigned. Any failure would result in the test stopping for manual verification before a restart signal was sent. Table 1 shows the distance of various locations from the plunger contact point. One important effect to be studied was the relation of distance from the point of maximum deflection of the PCB to the location of individual devices.

Location ID	Distance from Device to Plunger
17	1.47 mm
16	6.55 mm
27	8.05 mm
18	8.09 mm
5	8.93 mm
25	9.29 mm
26	11.15 mm
15	11.55 mm
19	13.31 mm

Table 1: Location ID vs. Distance from device to plunger

Discussion of Results

Two factors were studied during the course of this characterization effort. First was the relation between distance to point of maximum deflection with the onset of failures. Second was a comparative study for a given location (typically the one nearest to point of maximum deflection) among assemblies having different pad sizes on the PCB and on the device.

Results confirmed that the devices mounted nearest to the point of plunger application were the first to fail. This was followed by components failing in a sequence dictated by the distance to point of maximum deflection (which is same as the point of plunger application). Figure 7 shows the relation of distance from point of maximum deflection (1.5mm in this case) to the cycles required to cause device at that location to fail during flexural testing. Repeating the same for a 2mm maximum deflection showed the same trend of failures although at a slightly more accelerated pace.

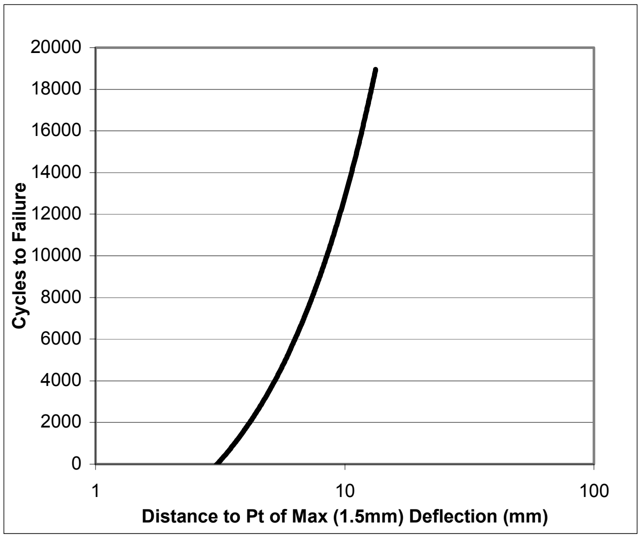

Figure 7: Relation between distance to point of maximum deflection and cycles to failure (0.17mm dia. Ball on 0.17mm dia. PCB pad)

A contour plot (Figure 9) shows the locations and zones on a PCB with the highest susceptibility to failures in applications involving flexing of the PCB. The PCB used was bolted at locations typically seen in a handset, resulting in the shape seen in the contour plot, i.e. contour plot is dependent on the PCB anchor locations and plunger point. The plunger application point is shown on the contour plot, located slightly off-center in relation to the center of the PCB. The slightly skewed shape of the contour plot is due to the bolting locations and method of bolting used, and the distance of a given device from the nearest bolt location. Based on these findings, it can be recommended that the region immediately around the area of maximum deflection should be avoided when placing very small wafer level devices during design and layout of the PCB. This would enhance the long-term application life of the devices in question.

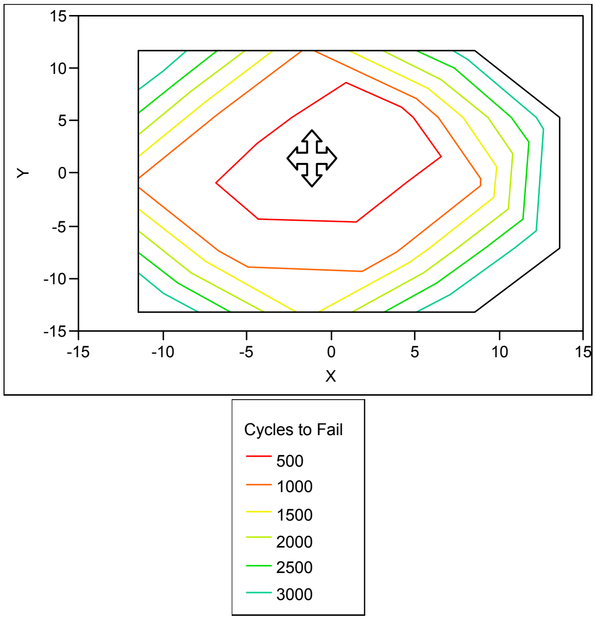

Figure 8: Contour plot showing cycles to failure regions in relation to the plunger location

In addition to the relation between distance to point of maximum deflection and its impact on cycles to failure, a relation was also established regarding the effects of using a device with a given ball size (or package pad size) with varying size of PCB pads. Three different combinations of solder bump/package pad size and PCB pad size were tested. The results of this test are shown in Figure 8. It demonstrated that using a small bump size (in this case 0.17mm ball size) with a much larger pad size on PCB (0.265mm in this case) had the most detrimental effect on the cycles required to cause failure. The test used both 1.5mm and 2mm maximum deflections (Figure 8 shows the chart for 2mm deflection), and both showed the same trend. It must be understood that this level of deflection is tested to achieve accelerated results in interest of test time.

Therefore it is important to follow the recommended 1:1 ratio between package pad/bump size, and the PCB pad size to avoid early failures in reliability testing and field failures. When PCB pad sizes are larger due to other design constraints and cannot be altered, a larger bump size is recommended to be used in order to approach the 1:1 recommended ratio.

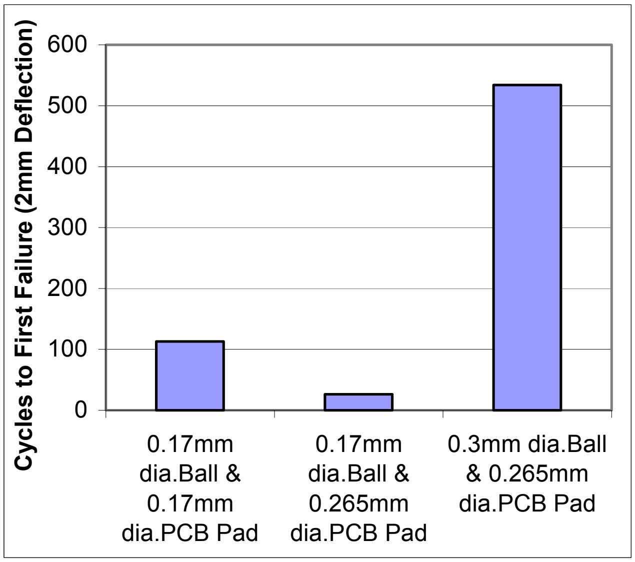

Figure 9: Effect of Ball size and Pad size interaction (with 2mm deflection at point of plunger contact)

Conclusion

Wafer level CSP products such as those assembled in the micro SMD packages are being increasingly used in handheld devices. Such applications have reliability requirements that comprise of not only the conventional environmental tests such as thermal cycling, bias testing, operating life, but also mechanical robustness tests like drop test, flex test, and bend/torsion test. Considerable effort is underway in the Industry and Academia to characterize packages under these tests to determine impact of design and process parameters on the reliability. Reliability in flexural testing, for example, is dependent on several variables such as location of the device on a given application PCB, potential mismatches between PCB pad size and package pad size on the package.

This paper described a test method developed to understand the influence of component location on PCB on the field reliability. The test method can be used to define component locations on the PCB to achieve highest life in flexural testing. This paper also discussed the effects of using a mismatched package bump pad size to PCB pad size, and identified the combination that will give the best results in repeated flexural bending environment.

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