

Board Level Reliability of Components with Matte Tin Lead Finish

L. Nguyen, R. Walberg, L. Zhou*, and T. Koh*
National Semiconductor Corp.
P.O. Box 58090 M/S 19-100
Santa Clara, CA 95052-8090

* National Semiconductor, Singapore

Abstract

Manufacturers, suppliers, and industry consortia have all been working towards a common acceptable drop-in solution for the standard eutectic tin lead. SnAgCu alloys are now expected to be the leading choice by the electronics industry. For instance, NEMI has recommended Sn3.9Ag0.6Cu as an industry standard for lead-free solder paste, with Sn0.7Cu for wave soldering. Similarly, SnAgCu alloys were also recommended for array packages. Unfortunately, there has been no recommendation for a lead-free finish for leaded packages, although these packages still constitute the largest portion of the worldwide semiconductor production. The IC suppliers had to struggle to evaluate the various lead-free finish options available (e.g., NiPd, SnBi, SnCu, SnAg, and matte Sn), and assess the resulting impact of the transition on their manufacturing logistics. Benchmarking indicated that two finishes have emerged to be leading contenders from such evaluation, namely, matte Sn and NiPd (1,2).

For a company to transition from tin lead to lead-free involves resolving a number of technical and logistics issues. This has been documented earlier for National Semiconductor (3).

This paper will report on the solder joint reliability of matte Sn used as a finish for leaded packages. Package selection, PCB design, solder wettability, selection of reflow profiles, and effect of reflow temperature will also be discussed.

The data showed the following:

- NiAu boards exhibited better wetting characteristics than did OSP boards.
- SnAgCu paste showed equal wetting onto SnPb and Sn components.
- No significant difference was seen between standard and linear reflow profiles in terms of wettability of SnPb and lead-free solder pastes.
- The 230°C profile did not completely reflow the lead-free solder pastes, although this did not translate directly to a weakening of the solder joints.
- Matte Sn components showed comparable board level reliability to that of SnPb.

Package Selection

The selection of packages for the board level qualification was based on the following criteria:

1. Include all lead configurations (gull wing, J-bend, and land contact area).
2. Represent a wide range of package body sizes.

The above criteria were decided upon because these factors have the greatest influence on the stress that the solder

joint experiences during board level temperature cycling. Table 1 shows the selected packages.

Table 1: Packages Selected for Board Level Qualification.

Package	Body Size (mm)	Lead Configuration
208L PQFP	28 x 28 x 3.4	Gull Wing
84L PLCC	29 x 29 x 3.7	J-Bend
20L PLCC	8.9 x 8.9 x 3.7	J-Bend
9L TO-263	10.2 x 8.7 x 4.6	Gull Wing
5L SC-70	1.25 x 2.0 x 0.9	Gull Wing
56L LLP	9 x 9 x 0.75	Land Contact
8L LLP	2.5 x 2.5 x 0.75	Land Contact

PCB Design and Board Level Assembly

Due to cost considerations, each PCB was designed to accommodate all package types on each of two sides. Thus, only a single PCB layout was needed. The PCB was of overall outer dimensions of approximately 150 mm x 225 mm and had edge connector fingers for insertion into mating connectors within a temperature cycling system. The PCB was designed to accommodate, on each side of the board, four PQFP 208L and PLCC 84L packages, 22 LLP 8L and LLP 56L packages, and 10 of each of the other package types. Figure 1 shows one side of the fully populated PCB.

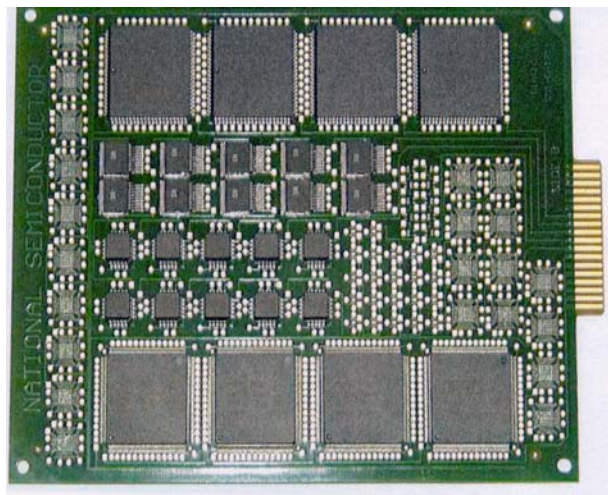


Figure 1: Fully Populated PCB.

The board material was FR4 (Tg approximately 120°C) of thickness 1.6 mm. Two types of board surface finishes were evaluated: electroless nickel-immersion gold (NiAu) and organic solder preservative (OSP).

There were 12 resistance loops per board for monitoring temperature cycling in-situ, with approximately 10 packages connected in series per monitoring channel. In addition, probe pads were added to the boards to assist in identification of failures.

The packages, consisting of Sn and SnPb lead finish, were assembled onto the boards with both lead-free solder paste (Sn3.5Ag0.7Cu) and SnPb eutectic solder paste. The solder pastes were of type 3 powder size with no-clean flux.

The PCB was populated using double-sided assembly. Components were glued as necessary to prevent displacement during the second side reflow. The assembled boards were inspected for any gross solder joint defects using an optical 20x stereo zoom microscope.

Solder Wetting Tests

The wettability of the Sn and SnPb components with both SnPb and lead-free solders was first assessed using a Multicore MUST II wetting balance. Four leaded package types were tested. The temperature of the SnPb solder was 235°C while that of the Sn3.5Ag0.7Cu was 260°C. A summary of the results is given in Table 2. Although Mil-STD-883 Method 2022 requires that the time to reach 2/3 of the maximum force is 1 second or less, this criterion was developed with SnPb components and SnPb solder.

Table 2: Wetting Balance Results.

Time (seconds) to achieve 2/3 of maximum force.

Lead finish:	Sn	SnPb	Sn	SnPb
Solder:	Sn3.5Ag0.7Cu		SnPb	
20L PLCC	0.73	0.27	1.25	0.35
84L PLCC	0.40	0.76	0.71	0.58
208L PQFP	0.16	0.16	0.79	0.15
9L TO-263	0.99	0.38	1.44	0.91

The results show that the wettability was poorest in the case of the Sn component with the SnPb solder, where two of the four packages failed the Mil-STD-883 1 second criterion. Considering the average wetting time over all four package types, the wettability was best for the SnPb component with the lead-free solder. The wetting times per package type were generally seen to increase with lead width and thickness, with the TO263 having the largest leads and the PQFP having the smallest.

In addition, the wettability of the SnPb and lead-free solder pastes on PCB contact areas was evaluated by printing the solder pastes onto PCBs and sending the unpopulated boards through reflow. In this study, two board finishes (NiAu and OSP), two reflow profiles (standard and linear), and two solder pastes (SnPb and Sn3.5Ag0.7Cu) were evaluated. The peak reflow temperature for both standard and linear profiles for the SnPb solder paste was 230°C, and for the lead-free solder paste was 240°C. The standard profiles had a leveling out of the thermal gradient in the preheat region, whereas the linear profiles had a near-constant slope throughout the thermal ramp. Results showed that good wetting was achieved in all cases except for the Sn3.5Ag0.7Cu paste with OSP boards, where both the

standard and the linear profiles resulted in incomplete wetting. Figure 2 shows this incomplete wetting.

Solder paste wetting tests were carried out on Sn and SnPb components by printing Sn3.5Ag0.7Cu solder paste onto a ceramic substrate and reflowing with a typical lead-free profile. All package types listed in Table 1 were included in this study.

Results showed that in all cases the lead-free solder paste was pulled up onto the leads and there was no solder remaining on the ceramic plate. Figure 3 shows that the lead-free paste equally distributed onto the leads of an 84L PLCC for both SnPb and Sn terminations.

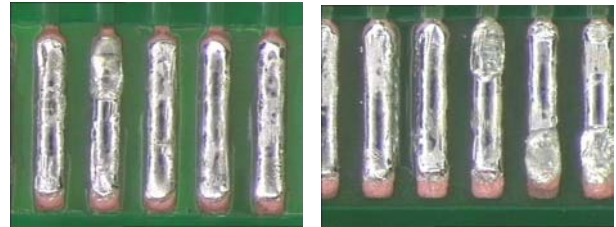


Figure 2: Incomplete Wetting of Sn3.5Ag0.7Cu Paste on OSP Boards. Left: Linear Profile. Right: Standard Profile.

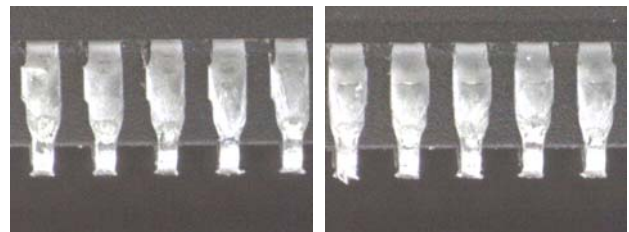


Figure 3: Equal Wetting of Sn3.5Ag0.7Cu Paste onto 84L PLCCs with SnPb (left) and Sn (right) Terminations.

Evaluation of Reflow Profiles

Two reflow profiles, standard and linear, were evaluated. For any single run with either profile, the peak reflow temperature was dependent on the solder paste under evaluation. Thermocouples were attached to the leads of several package types on a previously assembled board. In the case of the LLP packages, the thermocouple was attached from underneath through a hole drilled in the PCB to allow for the temperature to be measured on the ground pad of the package. The PCB assembly was then used to profile the oven for the following four cases:

1. Standard Profile for SnPb paste
2. Standard Profile for Sn3.5Ag0.7Cu paste
3. Linear Profile for SnPb paste
4. Linear Profile for Sn3.5Ag0.7Cu paste

Table 3 gives the parameters for these four profiles as measured on the 84L PLCC, while Figure 4 shows a general comparison between standard and linear profiles. Table 4 shows the variation among package types for the standard SnAgCu profile. Generally, the smaller packages were found to reach higher peak reflow temperatures.

Table 3: Reflow Parameters as Measured on the 84L PLCC.

Profile Type	Solder Paste	Time between 150 / 180 °C (sec)	Peak Temperature (°C)
Standard	SnPb	53	232
Standard	SnAgCu	58	242
Linear	SnPb	31	232
Linear	SnAgCu	29	242

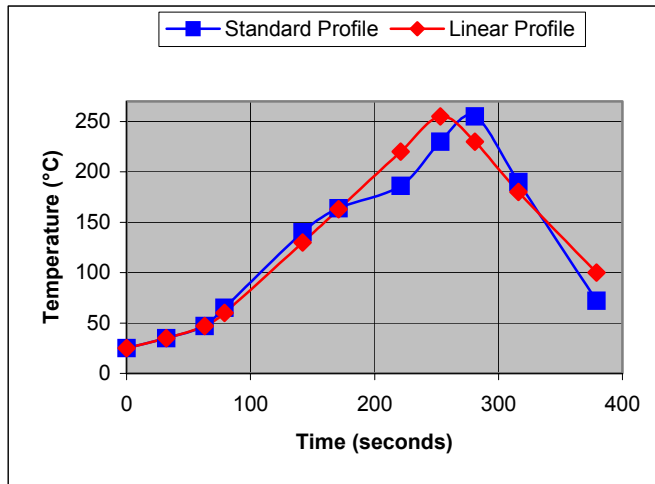


Figure 4: Comparison between Standard and Linear SnAgCu Profiles.

Table 4: Reflow Parameters for the Standard SnAgCu Profile.

Package Type	Time between 150 / 180°C (sec)	Total Time above 217°C (sec)	Peak Temperature (°C)
84L PLCC	58.6	63.7	241.8
5L SC-70	58.4	70.7	258.5
56L LLP	58.7	75.0	255.8
9L TO263	58.8	69.7	246.7
208L PQFP	62.2	61.8	242.8

Daisy chain test components representing several package types and two lead finishes were mounted onto the PCBs using both the standard and the linear profiles; both SnPb and lead-free pastes were represented, as were both NiAu and OSP boards. Resistances of the daisy chain loops were then measured. The resulting data showed that there was negligible difference in resistance measurements between (1) the standard and linear profiles, (2) the SnPb and Sn lead finishes, (3) the SnPb and SnAgCu solder pastes, and (4) the NiAu and the OSP board finishes.

A Dage tester was then used to measure solder joint strengths for the 208L PQFP. Parts were oriented in a horizontal position, and a single lead was pulled with a force applied perpendicular to the plane of the PCB. Results are

shown in Table 5, where each number represents the average of 6 pull measurements. The data shows no significant difference among the measured values. Specifically, no difference between standard and linear profiles was noted.

In order to further assess the differences between the standard and linear profiles, microsections of the 56L LLP solder joints were prepared. The cross sections revealed solder voids for both SnPb and SnAgCu pastes in the case of the linear profile but no discernable defect in the case of the standard profile. Figure 5 shows a sample of these cross sections.

Table 5: Pull Test Results (kg/lead) for the 208L PQFP.

Lead Finish	Profile	SnPb Paste		SnAgCu Paste	
		NiAu	OSP	NiAu	OSP
Sn	Standard	1.26	1.36	1.37	1.33
Sn	Linear	1.42	1.41	1.24	1.40
SnPb	Standard	1.46	1.35	1.28	1.31
SnPb	Linear	1.32	1.32	1.22	1.33

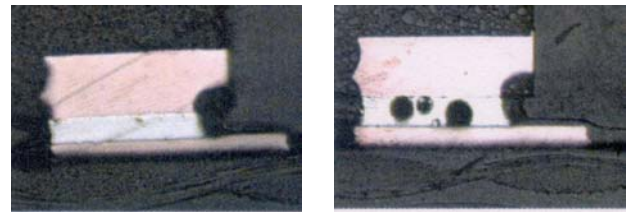


Figure 5: Comparison of SnAgCu Solder Joints in the 56L LLP. Left: Standard Profile. Right: Linear Profile.

Board Level Qualification

Because of the voids resulting from the linear profile for the LLP package, the standard profile was chosen for all of the board level qualification builds. All qualification builds were validated as follows:

- Top side paste printing was inspected for bridges, incorrect alignment and insufficient solder paste.
- Parts were inspected visually after SMT placement.
- After top side reflow, the joints were inspected visually and with X-ray.
- Electrical resistance of the top side loops was measured.
- The above validation was repeated for the bottom side assembly.

Daisy-chained parts were mounted on boards that were monitored for electrical continuity throughout the course of temperature cycling. In addition, the drop and vibration tests were done only on the LLP packages.

The temperature cycling was performed according to JEDEC JESD22-A104-B, Condition G (-40 to 125°C), with a 15 minute dwell time at the temperature extremes and at 1 cycle per hour. A 2-zone air-to-air temperature cycling system was used. Resistance measurements were carried out

at the maximum and minimum temperature extremes of each cycle. Testing was continued through 1050 cycles. For vibration tests, Mil-STD-810E was applied. Testing was carried out in three perpendicular axes with durations of 1 hour per axis. The drop test was done according to IEC 68-2-32, and involved dropping the PCB under acceleration due to gravity from 1.0 m onto a smooth, hard rigid steel surface. Four orientations were prescribed, with 2 drops per orientation. These orientations included: (1) vertical with the long edge downward, (2) vertical with the short edge downward, (3) horizontal with component side up, and (4) horizontal with component side down.

The sample sizes per package type for each of the board level reliability tests are given in *Table 6*.

Table 6: Sample Sizes per Leg for Reliability Tests. Legs included 2 Solder Pastes (SnPb and Sn3.5Ag0.7Cu), 2 Lead Finishes (SnPb and Sn), and 2 PCB Finishes (NiAu and OSP).

Package	Test	Sample Size per Leg
208L PQPF	TMCL	32
84L PLCC	TMCL	32
20L PLCC	TMCL	80
9L TO-263	TMCL	80
5L SC-70	TMCL	80
56L LLP	TMCL	80
8L LLP	TMCL	80
LLP 56L	Drop	24
LLP 8L	Drop	22
LLP 56L	Vibration	22
LLP 8L	Vibration	22

Qualification Results

The only package that experienced TMCL failures was the 56L LLP. These results are given in *Table 7*. In addition, *Table 8* shows the distribution of failures according to assembly materials and according to the side of the PCB on which failures occurred. All failures were classified as either open at hot, open at cold, or full open. A multimeter was used to probe the pads at intervals along daisy chain segments to determine which side of the component exhibited open circuit failure. Each LLP56 package had 12 segments to a daisy chain after assembly, so that the maximum number of solder joints per segment was six. After the approximate locations of the opens were determined, X-rays were taken to determine relative solder coverage. No observable difference in solder coverage between failed and good solder joints was discovered. The double-sided board design made the X-ray method difficult to use, since in many cases the joint on one side of the board was obscured by the joint or interconnections on the other side of the board.

Cross sections were then made of 23 of the failed parts. Failure analysis noted the following defects:

1. Extensive voids in the solder joints (*Figure 6*)

2. Poorly formed solder joints (*Figure 7*)
3. PCB pad lifting (*Figure 8*)

Table 7: TMCL Failures on 56L LLP.

Lead Finish	Solder Paste	Number of TMCL Failures	
		NiAu	OSP
Sn	SnAgCu	4	4
Sn	SnPb	2	0
SnPb	SnAgCu	3	4
SnPb	SnPb	4	4

Table 8: Distribution of 56L LLP TMCL Failures.

Total Packages failed: 25/640				
		No. of Failures	PCB Side A (2 Reflows)	PCB Side B (1 Reflow)
Paste	SnPb	10	1	9
	SnAgCu	15	7	8
	Total	25	8	17
PCB	NiAu	13	4	9
	OSP	12	4	8
	Total	25	8	17
Plating	SnPb	15	6	9
	Sn	10	2	8
	Total	25	8	17

Of the 23 LLP packages that were cross sectioned, 20 of them were found to have voids in the solder. Of these 20 parts, 11 of them contained voids significant enough to contribute to the failure. Of these 11 parts, 5 were with SnPb solder and 6 were with SnAgCu solder. Thus, the two solder pastes were seen to be equally likely to exhibit voids contributing to failure. In addition, it was determined that poorly formed solder joints contributed to 5 of the failures, with 4 of these being assembled with SnPb paste and 1 of them with SnAgCu paste. Finally, six of the parts had significant enough PCB pad lifting to contribute to the failures. All six parts were assembled with SnAgCu paste at peak reflow temperatures exceeding 255°C (see *Table 4*). It was also noted that in many cases there were voids (bubbles) in the FR4 material immediately below the lifted PCB pads. It may have been that the high peak reflow temperature associated with the SnAgCu paste resulted in the softening and outgassing of the PCB resin, forming bubbles that lifted the PCB pads. Finally, while most of the failures were equally distributed among the factors considered, it is interesting to note (*Table 8*) that side B of the PCB, which was reflowed only once, exhibited more failures than side A, which passed twice through the reflow furnace.

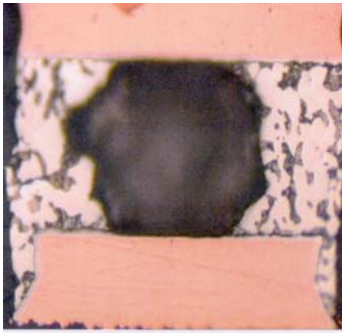


Figure 6: Void in Solder Joint. OSP PCB, SnPb component, SnPb Paste.

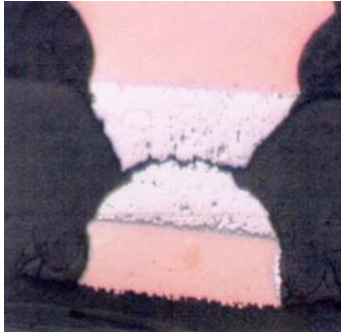


Figure 7: Poor Solder Joint. NiAu PCB finish, Sn Component, Sn3.5Ag0.7Cu Paste.

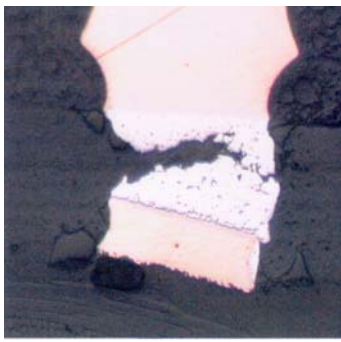


Figure 8: PCB Pad Lifting. NiAu PCB finish, Sn Component, Sn3.5Ag0.7Cu Paste.

As was the case for the TMCL results, the 8L LLP passed both the vibration and drop tests with no failures. However, the 56L LLP experienced failures as indicated in *Table 9*. In general these failures differed from the TMCL failures in that the joints all cleaved at the solder joint/PCB interface, whereas for the TMCL most of the failures were either through the bulk of the solder or at the solder/LLP pad interface.

At this point in the project it was discovered that the PCB land pattern for the 56L LLP was not constructed according to specifications. Rather than having a full solder mask opening over the center ground pad on the PCB, the solder mask opening was patterned with square openings in an array over the pad. Therefore, when the solder paste was applied to this pad, it could not spread out uniformly over this area. Had the PCB been constructed according to specifications, it is

believed that the package would have been pulled downward more evenly during reflow, resulting in more uniform solder coverage on the lead terminations. In turn, this would result in better overall solder joint integrity.

Table 9: Vibration and Drop Test Failures for 56L LLP.

Lead Finish	Solder Paste	PCB Finish	Failures	
			Vibration	Drop
Sn	SnAgCu	NiAu	0/22	0/24
		OSP	0/22	0/24
Sn	SnPb	NiAu	0/22	1/24
		OSP	0/22	0/24
SnPb	SnAgCu	NiAu	1/22	0/24
		OSP	0/22	0/24
SnPb	SnPb	NiAu	2/22	0/24
		OSP	6/22	0/24

Additional TMCL Data on the 56L LLP

Because of the above concerns, it was decided to redo the TMCL test on the 56L LLP package using a PCB designed with a full solder mask opening over the ground pad. This is the prescribed board design for an LLP, so it would also provide for more realistic data. Rather than being monitored continuously, the boards were removed at 750 and 1050 cycles for hand testing. The TMCL results are shown in *Table 10*.

The results show a substantial improvement over the first set of data. The cross-sections that were taken showed more uniformity in solder joint formation. *Figure 9* is representative of the solder joints that were seen among the various legs of the evaluation. The only failures occurred in the leg with SnPb components, SnAgCu paste and OSP boards. All 16 failures were located at corner pins. *Figure 10* shows one of these failures, where the solder separated from the component contact area. This failure mode was typical among the 16 failures. It was later found that contamination on the package contacts contributed to these failures.

Table 10: Second Set of TMCL Results for 56L LLP.

Lead Finish	Solder Paste	PCB Finish	Failures	
			750 TMCL	1050 TMCL
Sn	SnAgCu	NiAu	0/98	0/98
		OSP	0/96	0/96
Sn	SnPb	NiAu	0/100	0/100
		OSP	0/99	0/99
SnPb	SnAgCu	NiAu	0/99	0/99
		OSP	2/99	16/99
SnPb	SnPb	NiAu	0/100	0/100
		OSP	0/95	0/95

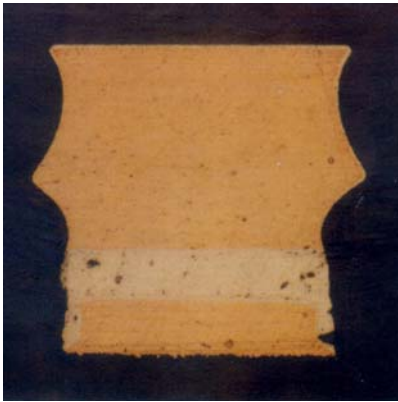


Figure 9: Good Solder Joint. SnPb Lead Finish, SnAgCu Solder Paste, OSP Board.



Figure 10: Failed Solder Joint. SnPb lead finish, SnAgCu Solder Paste, OSP board. This is a Corner Pin Located Adjacent to that shown in Figure 9.

Effect of Reflow Temperature on Solder Joint Integrity

As a related effort, an experiment was designed to determine the effect of reflow temperature on solder joint integrity. The packages that were used in this evaluation included the 5L SOT-23, the 24L TSSOP, and the 20L SOIC. All components were plated with matte Sn. The solder pastes that were evaluated included Sn3.0Ag0.5Cu and Sn3.9Ag0.6Cu. The boards were designed with perforations between the land patterns such that after board mount, each mounted package could be singulated to enable attaching the punched out PCB section to the mounting jig on the Instron tester. The mounting jig was designed to hold the PCB section at a 45° angle. An 8-mil wire was threaded through a single lead and then clamped to a small fixture affixed with a hook to the Instron load cell.

Reflow was done using a standard profile with peak reflow temperatures of 230°C, 240°C, and 250°C. For each of two solder pastes and each of the three peak reflow temperatures, five parts of each package type were mounted onto the boards. The Instron was then used to collect the pull test data. Four leads were pulled from each TSSOP and SOIC package. Only one lead from each SOT-23 package was pulled. The resulting data is shown in Table 11. The data show that there was no significant difference in solder joint pull strength among the three peak temperatures that were

investigated. Also, there was no significant difference in pull strength between the two solder pastes evaluated.

In addition, one SOIC part from each of six legs was cross sectioned across a pair of solder joints and inspected using an optical microscope. These cross sections revealed that neither of the two solder pastes completely reflowed at 230°C, whereas both solder pastes completely reflowed at 240°C and 250°C. This could best be seen by focusing inside of a small void in the solder. The legs that were completely reflowed (240°C and 250°C profiles) revealed a bright metallic inner surface to the void, whereas the legs that were incompletely reflowed (230°C profile) revealed a dull dark inner surface to the void (see Figure 11).

Conclusions

This study has shown that matte Sn components exhibit comparable board level reliability to that of SnPb. In addition, the following was concluded:

- NiAu boards exhibited better wetting characteristics than did OSP boards.
- SnAgCu paste showed equal wetting onto SnPb and Sn components.
- No significant difference was seen between standard and linear reflow profiles in terms of wettability of SnPb and lead-free solder pastes.
- The 230°C profile did not completely reflow the lead-free solder pastes, although this did not translate directly to a weakening of the solder joints.

Table 11: Pull Test Results.

Package	Peak Reflow Temperature (°C)	Pull Test Averages (kg/lead)	
		Sn3.0Ag0.5Cu	Sn3.9Ag0.6Cu
SOT-23	230	1.33	1.45
	240	1.27	1.50
	250	1.27	1.52
TSSOP	230	0.90	0.81
	240	1.05	1.15
	250	1.05	1.03
SOIC	230	2.39	1.87
	240	1.83	1.87
	250	1.96	1.86

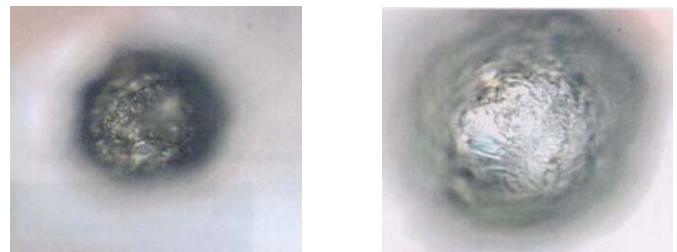


Figure 11: Inner Surface of Void from 230°C Reflow (left), and from 240°C Reflow (right).

Acknowledgments

The authors would like to thank R. Martin (Package Technology Group) and A. Khan (Quality and Reliability) for their assistance. Thanks are also extended to Gintic, Singapore, for their efforts.

References

1. *IPC Works 1999*, October 23-28, 1999, Minneapolis, MN; *IPC Works 2000*, September 9-14, 2000, Miami, FL; *IPC/JEDEC Int. Conf. On Lead-Free: Electronic Components and Assemblies*, May 1-2, 2002, San Jose, CA.
2. "Lead-Free – Fantasy or Fact", *MEPTEC 2000*, June 14, 2000, Sunnyvale, CA; "Summit on Lead-Free Solder Implementation," *MEPTEC 2001*, January 10, 2001, San Jose, CA; "Lead-Free Solder Implementation Summit," *MEPTEC 2001*, August 30, 2001, Sunnyvale, CA.
3. Nguyen, L., Walberg, R., Lin, Z., Koh, T., Bong, YY, Chua, MC, Chuah, S., and Yeoh, JJ, "A Structured Approach To Lead-Free IC Assembly Transitioning," *27th IEMT Symposium*, pp. 215-222, July 17-18, San Jose, CA (2002).