

The Effect of Electromigration on Eutectic SnPb and Pb-free Solders in Wafer Level-Chip Scale Packages

Joanne Huang¹, Stephen Gee², Luu Nguyen², King-Ning Tu¹

¹*Department of Materials Science and Engineering, University of California - Los Angeles, Los Angeles, CA 90095-1595*

²*National Semiconductor Corporation, Santa Clara, CA 95051*

Introduction

Reliability is an ongoing, crucial part of the microelectronics industry as companies continue to increase the population of I/O connections and shrink package dimensions. As outlined in the International Technology Roadmap for Semiconductors¹ (ITRS), this trend causes increased current density in solder joints, making electromigration the limiting reliability factor in high density packages. Electromigration leads to serious reliability factors such as joule heating and solder/silicon interface voiding which ultimately lead to failure. In this experiment, both the electrical and thermal effects due to electromigration are studied with eutectic 63Sn-37Pb (e-SnPb) and Pb-free 95.5Sn-4.0Ag-0.5Cu (SAC 405) solder bumps in Wafer Level-Chip Scale Packages.

Wafer Level-Chip Scale Packaging² (WL-CSP) is fabricated efficiently, completed directly on the wafer, and has a true chip size due to the wafer level processing. The test chip layout used for this experiment consists of a 6-by-6 array of 300 μm diameter solder bumps with a pitch of 500 μm , tested at current densities ranging from $3.36 \times 10^3 \text{ A/cm}^2$ to $3.67 \times 10^3 \text{ A/cm}^2$ in an ambient temperature of 50°C. The large amount of joule heating and the package junction-to-air factor leads to actual die temperatures about 80% of the solder's melting temperature.

The discussion for electrical data analyzes the parameters of Black's Equation used in estimating failure time.³ The thermal factors discussed here will shed light on unexpected failure at low temperatures and even solder melting during electromigration testing.⁴

Background

Electromigration is atomic diffusion caused by a combination of high temperature and high current conditions where the momentum of the electrons is transferred to the atoms. This phenomenon, with respect to solder balls, correlates to several failure mechanisms such as

solder/silicon interface voiding as a result of current crowding, as well as the formation of intermetallic compounds and under-bump metallization consumption caused by migrated phases.

Black's electromigration study using Aluminum lines³ gives the standard by which the Mean-Time-To-Failure (MTTF) is predicted, shown in Equation 1.

$$MTTF = Aj^{-n} \exp\left(\frac{Q}{kT}\right) \quad (1)$$

Where A is a constant, j is the current density, n is a model exponent for current density, Q is activation energy, k is Boltzmann's constant, and T is the bump temperature.

One of the most significant differences between the electromigration in Aluminum lines and electromigration in solder balls is the non-uniform current density that occurs within the solder ball. The uneven distribution can be attributed to current crowding in which a large portion of the current enters the solder bump at the nearest corner. The concentration of high current and high temperature at this corner causes the formation of voids. This continues across the entire solder/silicon interface and leads to failure.⁵ In an effort to better fit Black's Equation to solder bump electromigration failure, data has been fit to quantify the current density exponent and activation energy.^{5,6}

Another serious issue in the study of electromigration is the localized heating that takes place. In a previous study, the die temperature was assumed to be approximately equal to the ambient or oven temperature⁷; while other studies have performed crayon tests to roughly measure die temperature.⁵ However, the thermal side of electromigration is an issue that needs further examination.

Experimental

In examining the electromigration reliability of Wafer-Lever Chip Scale Packages, a test chip was designed to not only provide electrical data

but die temperature as well. The resistance was measured across 10 pairs of solder bumps in a daisy chain layout to determine electrical failure and temperature sensors on the test chips allow for in-situ monitoring of the die temperature through resistive I^2R heating. The electron flow for one side of bumps is shown in Figure 1 and the locations where voiding occurred due to electromigration are circled in green at bumps 1, 3 and 5.



Figure 1. Cross-sectional SEM image. Electron flow (green) for one side of test die.

Each test board contained four test die and the data from each board was extracted using a system of 50 pin D-sub and 96 pin DIN connectors wired through PC Board edge card connectors (shown in Figure 2).

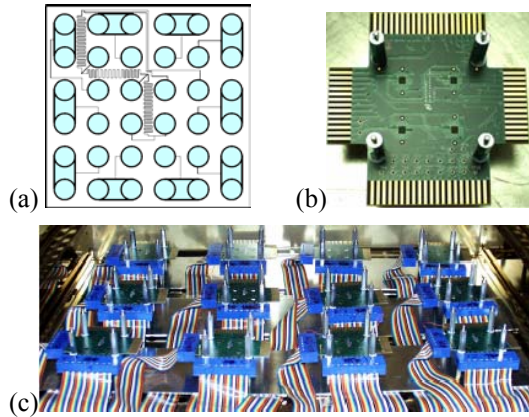


Figure 2. (a) Test Chip Design showing solder bump pairs and serpentine resistors. (b) Test board with four WL-CSP test die. (c) Twelve test boards inside the oven with connectors.

The computerized data acquisition and switching system allowed for several boards to be tested at once thereby allowing the simultaneous testing of the eutectic SnPb solder and the SAC 405 solder at similar conditions. The experiment parameters are shown in Table 1 below.

Table 1. Experiment Parameters

Current (A)	Solder Bump Composition	Under-Bump Metallization	Current Density (A/cm^2)
1.65	63Sn-37Pb	Al/Ni(V)/Cu	3361
1.7	63Sn-37Pb	Al/Ni(V)/Cu	3463
1.65	SAC 405	Al/Ni(V)/Cu	3361
1.7	SAC 405	Al/Ni(V)/Cu	3463
1.8	SAC 405	Al/Ni(V)/Cu	3667

The solder balls in this wafer-level chip scale package are 300 μm in diameter with a 500 μm pitch. The under-bump metallization (UBM) consists of Al, Ni(V) and Cu whose thicknesses are 1 μm , 0.32 μm and 0.8 μm , respectively. These values are consistent in test die for both eutectic SnPb and SAC 405 solder bumps.

The failure criterion is satisfied when the change in the bump resistance exceeds 15%. Changes in the resistance less than 15% provided an early warning signal to imminent failure.

Results and Discussion

In the past, assumptions were made on the actual die temperature but with the Aluminum serpentine resistors, the die temperature and the contributing thermal factors could all be precisely quantified. The calculation of the die temperature included a junction-to-air packaging factor, θ_{ja} (Equation 2a). The θ_{ja} of each die varies depending on the position of the die on the test board; therefore each die position was calibrated to give the correct θ_{ja} value (Figure 3).

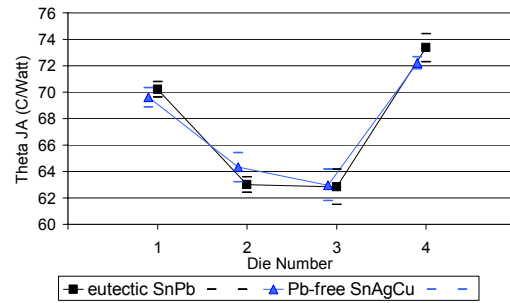


Figure 3. Theta-ja junction-to-air packaging factor for each of the four die on the test board

The die temperature was calculated using Equation 2 (below). The joule heating and package θ_{ja} factor were included in determining the final die temperature. These additional factors added a significant amount to the final temperature of the test die. The resistance, R , is the total resistance of the 20 bumps with each solder bump/interconnect resistance being 26 milliohms. T_f is the final die temperature, T_0 is the beginning die temperature and I is the current applied to the sample.

$$\theta_{ja} = \frac{T_f - T_0}{I^2 R} \quad (2a)$$

$$\Delta T = \theta_{JA} \cdot P = \theta_{JA} \cdot I^2 R \quad (2b)$$

$$T_{die} = T_{oven} + \Delta T \quad (2c)$$

In this case the oven temperature was 50°C and the maximum die temperature under our test conditions was aimed at 80% of the melting temperature of the solder, or 149°C for eutectic SnPb and 174°C for SAC 405. Estimated test temperatures are listed in Table 2.

Current (A)	Current Density (A/cm ²)	Estimated Testing Temperature
1.65	3361	139-154°C
1.7	3463	145-160°C
1.8	3667	156-174°C

Including all the thermal factors was crucial in determining the test conditions. Without the junction-to-air packaging factor, the die temperature is severely underestimated by more than 50°C.

In the results, the temperature increased relative to the resistance increase. Through cross-sectional analysis, the amount of voiding at the solder/silicon interface current crowding location can be connected to both the increase in resistance and temperature.⁸ As current crowding takes place at the corner of the bump (see Figure 4), not only is the current displaced each time a void forms at the interface, but the ability of the solder bump to dissipate heat is diminished. Subsequently as more and more voids form, the total contact area is decreased, there is less area for the heat to transfer through, thus producing an increase in the die temperature.

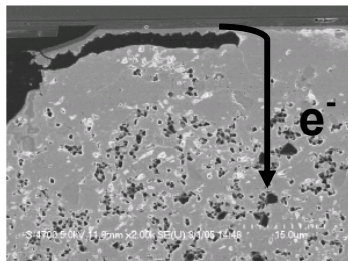


Figure 4. Close-up of SnAgCu Bump 1. Solder/Silicon Interface Voiding taken by SEM.

As expressed in Black's Equation, electromigration reliability is characterized by the Mean-Time-To-Failure (MTTF). Table 3 shows the MTTF for both eutectic SnPb and Pb-free SAC 405 per the testing conditions outlined in the previous section. From this we can see the MTTF for failed bumps at a current density of 3.36×10^3 A/cm² (corresponding to 1.65 A), the SAC 405 samples had over 1.5 times longer Mean-Time-To-Failure than the SnPb samples

and for 3.46×10^3 A/cm² (corresponding to 1.7 A), the MTTF for SAC 405 was over 2.5 times more than for SnPb.

Current (A)	Solder	MTTF (hours)	Average Temp. at Failure (°C)	No. of Failed Bump Pairs
1.65	e-SnPb	1866	147	16
1.7	e-SnPb	1069	155	42
1.65	SAC 405	4756	134	3
1.7	SAC 405	1754	155	25
1.8	SAC 405	859	160	56

In addition to the Mean-Time-To-Failure, the activation energy parameter within Black's Equation was also calculated using the data (see Figure 5). The activation energy for the SAC 405 solder was found to be about 0.8 eV. The data is still being collected to calculate the activation energy for eutectic SnPb.

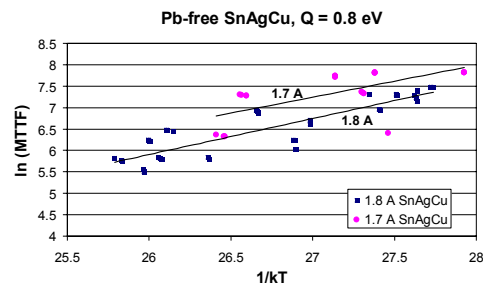


Figure 5. SAC 405 Activation Energy.

The difference in this study of electromigration compared to previous studies consists of more than its ability to accurately measure the die temperature. A comparison of MTTF for flip chip and Wafer-Level Chip Scale Packages can be made. Under similar testing conditions for eutectic SnPb⁷, the MTTF for the WL-CSP package is approximately three times the MTTF for the flip-chip package. Notably, the diameter of the WL-CSP solder bump is about three times greater than the diameter of the WL-CSP bump diameter. A linear scaling relation can be deduced. The significant thermal effects of the WL-CSP tested in this experiment, however, limited the testing conditions to an order of magnitude less than typical testing conditions for flip-chip packages. Therefore, the majority of studies for flip-chip electromigration were not able to be directly compared to this study.

The thermal factors in WL-CSP are more significant than in flip-chip packaging. Studies in flip-chip packages^{6, 7} observe voiding across

the entire solder/silicon interface, while in the WL-CSP samples, the voiding only occurred in less than 12% of the bump area before exceeding the failure criteria⁸. Moreover, the failure criteria in most flip-chip packages is a resistance change of 300% but the thermal issues in the WL-CSP package required the failure criteria to be set much lower in order to preserve the integrity of the data from the other die on the test board as well as preventing solder melting and fire. Although the thermal effects in WL-CSP are more than in flip-chip packages, the factors introduced in this paper should still be considered and play a telling role in testing flip-chip packages.

Conclusions

The test setup used in this experiment allowed for high batch size statistics in determining the electromigration induced Mean-Time-To-Failure and the activation energy for Pb-free SnAgCu. Although the current densities tested in these Wafer-Level Chip Scale Packages was not extreme in comparison to previous studies done on flip chip packages, the die temperature was the dominant factor as joule heating and the junction-to-air packaging factor increased the die temperature significantly above the oven temperature. An increase in the temperature directly correlated to an increase in the bump resistance both of which can be attributed to electromigration induced voids at the solder/silicon interface. A scaling relation of the mean-time-to-failure between flip-chip packages and wafer-level chip scale packages relates the bump diameter to failure times linearly.

Future Work

The current pitch of the solder bumps is 500 μm but testing has begun on 400 μm pitch bumps to observe any changes in terms of heat dissipation and mean-time-to-failure.

There is a clear correlation of the voided solder/silicon interface to the increase in the resistance of the solder bump as well as an increase in the temperature. A planar in-situ observation of the nucleation and propagation of voids while the solder bump is being applied with current will provide accurate data in terms of viewing the progress of the voids across the solder/silicon interface.

Acknowledgments

The authors would like to thank the Semiconductor Research Corporation/Education

Alliance with National Semiconductor Corporation Master Scholarship Program for their continued support, as well as SRC Contract NJ-1080.

References

- [1] International Technology Roadmap for Semiconductors, 2004 Update, Assembly and Packaging, pg. 3.
- [2] N. Kelkar, R. Mathew, H. Takiar, L. Nguyen, IEEE Trans. On Advanced Packaging, special issue on Wafer Level Packaging, vol. 23, no.2, 227-232, May 2000.
- [3] J.R. Black, IEEE Transaction on Electronic Devices, Ed. 16 (4), 338, 1969.
- [4] J.W. Nah, J.O. Suh, K.N. Tu, Journal of Applied Physics, 98, 013715, 2005.
- [5] W.J. Choi, E.C.C. Yeh, K.N. Tu, Journal of Applied Physics, vol. 94, no. 9, 5665-5671, 2003.
- [6] S. Brandenburg and S. Yeh, Surface Mount International Conference and Exposition, SMI 98 Proceedings, 1998.
- [7] J.D. Wu, P.J. Zheng, K. Lee, C.T. Chiu, J.J. Lee, IEEE 41st Annual International Reliability Physics Symposium, 132-139, 2003.
- [8] S. Gee, J. Huang, K.N. Tu, N. Kelkar, Proceedings of InterPACK 2005, IPACK2005-73417.