Mean Time To Failure in Wafer Level-CSP Packages with SnPb and SnAgCu Solder Bumps

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ABSTRACT

In this test setup, embedded die surface temperature sensors are used to assess device electromigration performance using a high precision, high density, resistance measurement system. Solder bump failures are found to result from voiding at the UBM/solder interface where CuSn intermetallic formation and vacancy pileup are observed. The driving mechanisms for electromigration induced voiding are determined experimentally through activation energies measurements in eutectic SnPb and SnAgCu solders.

Recommendations for how to measure electromigration in WL-CSP (Wafer Level-Chip Scale Package) solder bumps are also presented. Based upon an analytic model for calculating the resistance change due to solder bump voiding, it was determined that the fractional change in bump via opening should result in an absolute change in resistance, which should be independent of solder bump diameter.

Key Words: Resistivity; Sheet Resistance; Solder Resistance; Eutectic SnPb; SnAgCu; Lead Free; Electromigration; Temperature Sensor.

INTRODUCTION

In these experiments, electromigration test data on eutectic SnPb and SnAgCu (SAC 405) solders are fit to Black's *Eq. (1)* in order to determine activation energies for failure. This data set is compared with the activation energies for material transport to infer the mechanism by which vacancy pileup in the opposite direction occurs. Black's equation is given by:

Eq. (1)

$$MTTF = Aj^{-n}\exp\left(\frac{Q}{kT}\right)$$

where MTTF is the Mean Time To Failure, A is a constant, j is current density, n is a model parameter for current density, Q is the activation energy, k is Boltzmann's constant, and T is the average bump temperature [1]. Since Black's equations assumes isothermal testing conditions, for each data point collected, it was found that a failure criterion associated with the onset of failure was preferable to one closer to a catastrophic failure criterion.

This damage onset failure criterion is useful when working at lower current densities, where the time between void nucleation and catastrophic failure can be long, and factors such as Joule heating can become more pronounced. This can complicate data interpretation, because activation energies estimates could be due to contributions from multiple sources.

Measurement of solder bump electromigration, and the interpretation of electrical data, is also complicated by the fact that changes in solder bump resistance are many orders of magnitude smaller than the interconnect resistances used to make the measurements. Therefore, the usage of high precision, 4-point Kelvin resistance measurement techniques are invaluable in increasing sensitivity to the minute changes resulting from "pancake type" void growth at solder/UBM interfaces. An analysis of the sources responsible for resistance change and their absolute magnitudes, is useful in filtering the data to emphasize sensitivity to void growth characteristics.

EXPERIMENTAL SETUP

In these experiments, multiple solder bumps were wired in series in order to maximize the number of solder bumps tested on each die. This means that I^2R Joule heating will be multiplied in direct proportion to the number of bumps in the daisy chain. In actual IC devices, current carrying solder bumps are wired in parallel, which tend to reduce the I^2R Joule heating effects.

The test chip used in these experiments employs a simple one layer metal, 36-bump layout. The outer 20 bumps are wired in a daisy chain using wide metal traces to carry the high currents required to accelerate electromigration damage (*Figure 1*). The inner 16 solder bumps are used to access voltage sense nodes on the perimeter solder bump array and to connect to three temperature sensors on each die. Temperature is measured based upon the temperature coefficient of resistance of aluminum serpentine resistors which are visible on the upper left corner of the test chip die, *Figure 1*.

A key component of these experiments is the PC board, *Figure 2*, which is designed with edge card connectors for easy hookup to an automated measurement system capable of simultaneous data collection on 12 PC boards. Since each PC board holds 4 test dies, the automated test system has a total data handling capacity of 48 test dies. The test system has been running continuously for the last year, collecting data on 960 solder bumps and 144 temperature sensors every 15 minutes. The solder bump resistance measurements are made in groups of 5 solder bumps, from each of the 4 die edges, for a total of 240 daisy chain resistance measurements every 15 minutes [2].

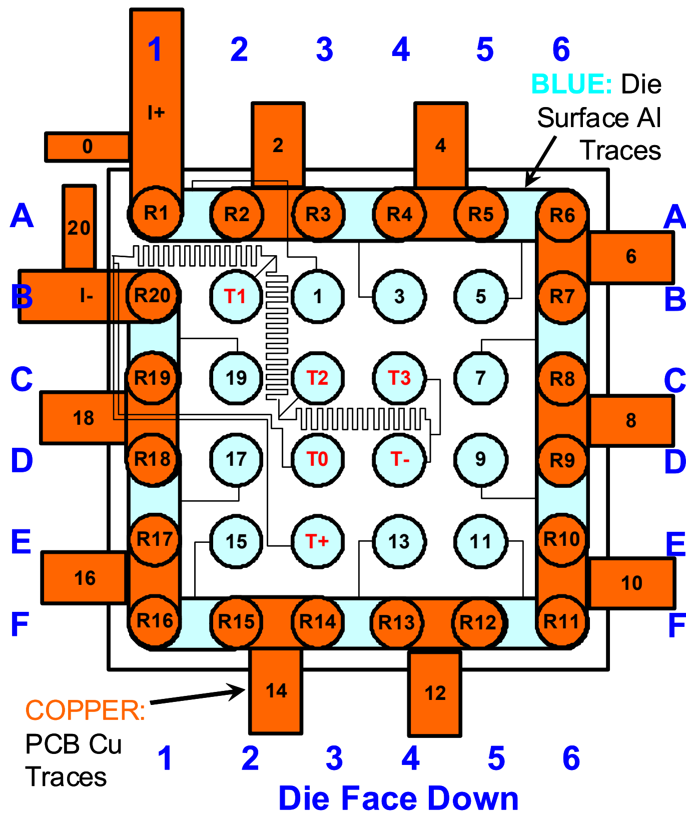

Figure 1 Schematic drawing of the bump electromigration test chip (blue) and the PC board interconnect traces (orange).

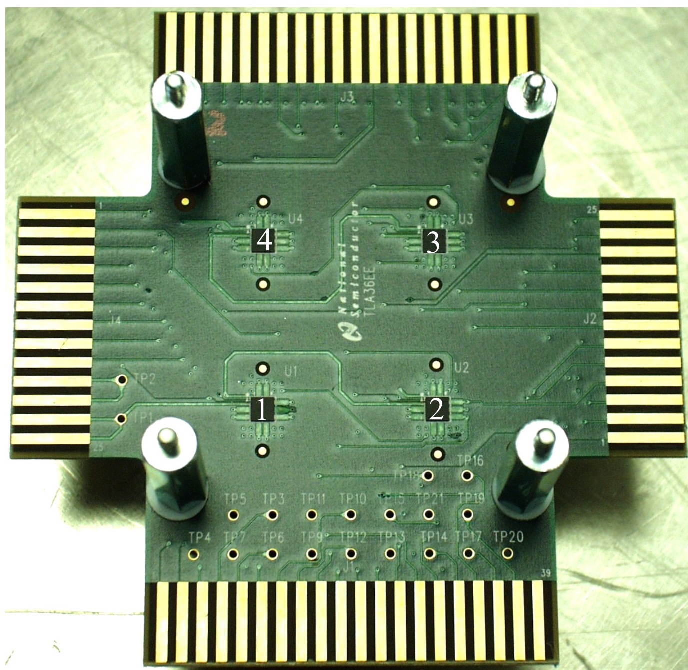

Figure 2 Photograph of the electromigration test board (8.9 mm x 8.9 mm) showing four mounted test chips.

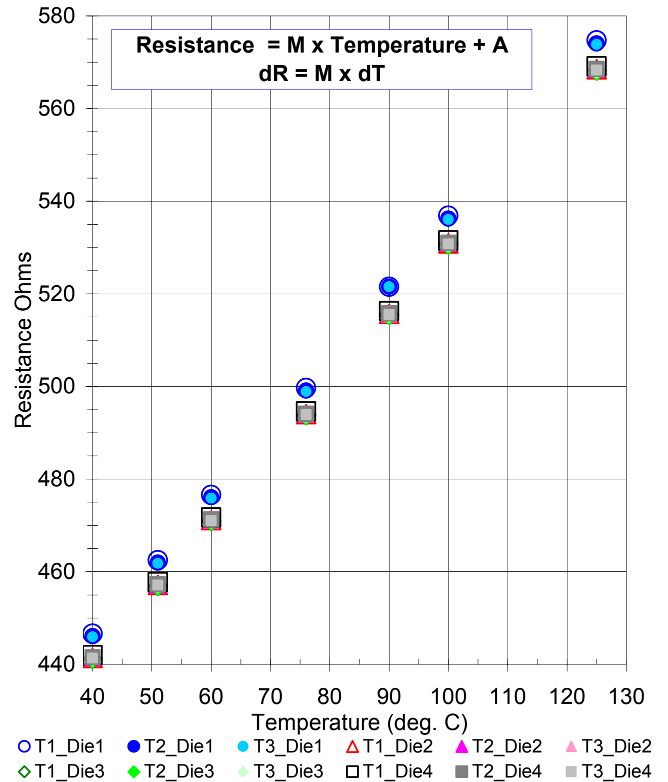

Figure 3 Plot showing linearity in the 12 temperature sensor measurements on one board.

Temp Sensor	M ohms per °C	A ohms at 0°C	R^2 fit to a straight line
1	1.5096	385.77	0.9999
2	1.5093	385.28	0.9999
3	1.5093	385.13	0.9999
4	1.4972	381.05	0.9999
5	1.4970	381.01	0.9999
6	1.4971	380.98	0.9999
7	1.4964	380.87	0.9999
8	1.4953	380.57	0.9999
9	1.4953	380.52	0.9999
10	1.4977	381.6	0.9999
11	1.4964	381.22	0.9999
12	1.4958	381.05	0.9999

Table 1 Least square fit to a straight line in the 12 temperature sensors on one board.

In order to accelerate failure and to fit the data to Black's Eq., die surface temperatures ranging from 125°C to 190°C were collected. A key experimental constraint in this experiment design is that the edge card connectors and ribbon cable wiring, which are only capable of extended operation at 100°C (80°C

for multicolored ribbon cable). Therefore, some sort of I^2R Joule heating is a necessary constituent of the test design.

As can be seen in *Figure 3* and *Table 1*, the temperature sensor resistance measurements can be fit to a straight line with a R^2 value of 0.9999. Due to this linearity, all subsequent test boards were calibrated at 40°C and 80°C. The slopes, M, and the intercepts, A, are determined for each serpentine resistor. The slope, M, corresponds to dR/dT, the change in resistance for a 1°C change in temperature. The intercept, A, corresponds to the projected trace resistance at the reference temperature of 0°C.

EXPERIMENTAL RESULTS

In these experiments, the failure criterion chosen was a 15% change in resistance in a daisy chain of five solder bumps. *Table 2* shows the electromigration test conditions used in these experiments. *Figure 4* shows the time to failure for the SAC 405 solder. As can be seen in this figure, for the test conditions used, temperature has a much more influential effect than current density. The red curve shows the fit to Black's eq. for the large ball, 1.8 A PC boards and corresponds to an activation energy of Q = 0.84 eV/atom. Dimensions for the solder bumps are shown in *Table 3*.

Current (A)	Current Density (A/cm^2)			
	Large Bump	Solder	Small Bump	Solder
1.8	3667	SAC 405	5197	-
1.7	3463	Pb63Sn or SAC 405	4908	SAC 405
1.65	3361	Pb63Sn or SAC 405	4764	SAC 405

Table 2 Electromigration test conditions.

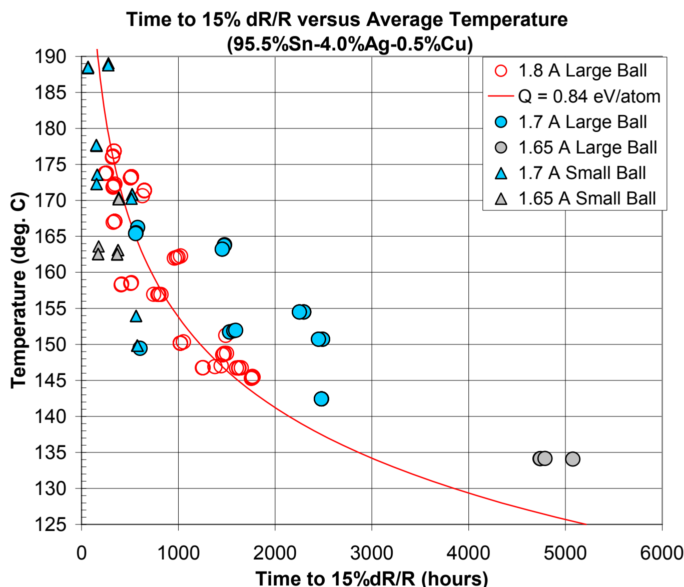

Figure 4 Plot showing the time to 15% dR/R in lead-free solder bumps. At 1.8A, the activation energy was 0.84 eV/atom.

Figure 5 shows the resistance and temperature data for four dies on one eutectic SnPb PC board. At about the 2000 hour time point, die #4 (green) exceeded the 15% dR/R failure criterion. After jumper wire shorting across the failed die, the die surface temperature drops from 150°C to about 75°C (orange). This time point corresponds to a 5°C to 10°C drop in temperature on the neighboring test die (red, violet and pink) and a slight drop in the measured bump resistance (black, blue and silver). This suggests that the statistics could be improved if temperature compensation for the interconnect resistances is done. At the 3300 hour time point, Die #1 fails (black), and similar temperature drops, in the remaining two die, are observed after jumper wiring across Die #1.

While failure has not yet occurred on die numbers #2 and #3, a monotonic increase in resistance can be observed. The dashed lines can be followed to the 15% dR/R resistance level to make predictions regarding the expected failure time point at these lower die temperatures. Using these dotted lines it is predicted that at 123°C Die 2 (blue) should fail at about 9700 hours. Die 3 (silver) is predicted to fail after 8300 hours at 125°C. Black's Equation fits to the 1.65 A eutectic SnPb PC board, including the low temperature projections, are shown in *Figure 6*. The slope in this chart gives an activation energy of 1.08eV. A plot of the 1.65A data, the low temperature failure predictions, in addition to all of the 1.7A eutectic SnPb data collected to date are shown in *Figure 7*.

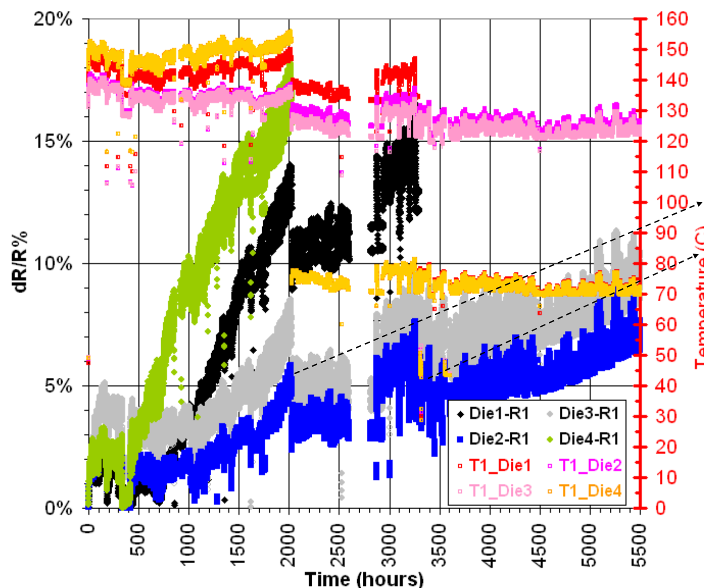

Figure 5 Resistance and temperature data for one eutectic SnPb board at 1.65 Amp.

The activation energies previously reported for flip-chip packages range from 0.5 to 0.9 eV/atom for both eutectic SnPb and SnAgCu, [3][4]. The temperatures of these packages were estimated to be within 3°C of the ambient temperature. For the eutectic SnPb and SAC 405 in these studies, the activation

energies are due to a combination of lattice diffusion and grain boundary diffusion. In the investigation of eutectic SnPb, Gupta *et al.* showed the interlamellar, grain boundary diffusion of Sn and Pb in eutectic SnPb solder is approximately 0.8 eV/atom [4]. The failure mechanism in these studies is identical to ours, voiding at the solder/UBM interface.

The activation energy of SAC 405 is in good agreement with a previous study by Choi *et al.* [4]. The previously reported values for eutectic SnPb, however, are in the range of 0.5 – 0.8 eV/atom as mentioned above. Notably in those studies, the die temperature was reported as approximately the ambient temperature although the homologous (T/Tm) is greater than 0.5, is not nearly as close to the melting temperature as our tests have been.

Since the testing takes the wafer level-chip scale package to temperatures near the melting temperature for the eutectic SnPb solder, lattice diffusion takes place. This explains our 1.1 eV/atom as previous studies activation energies have been a combination of lattice and grain boundary diffusion at operating temperatures much lower than in our testing. Gupta *et al.* clearly state that the activation energies of Sn and Pb in eutectic SnPb solder by lattice diffusion, are approximately 1.0 eV/atom [4].

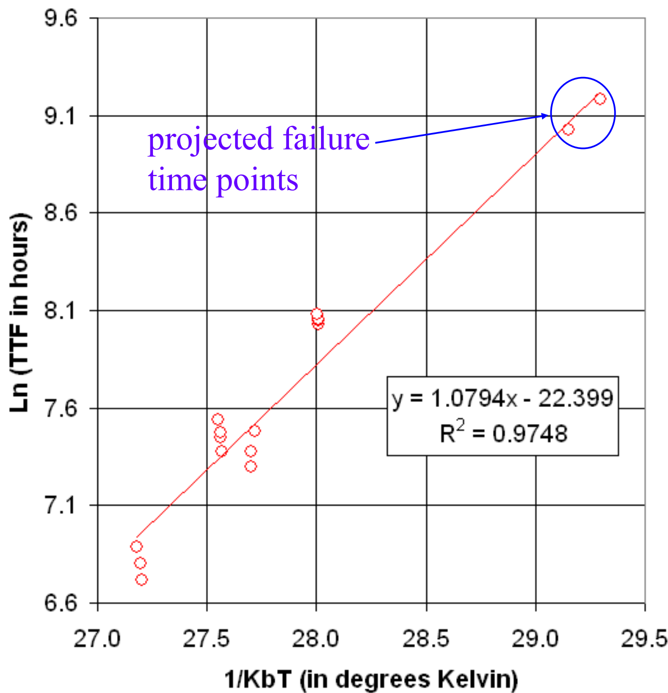

Figure 6 Time To Failure in 1.65 A eutectic SnPb solder bumps showing an activation energy of 1.08 eV.

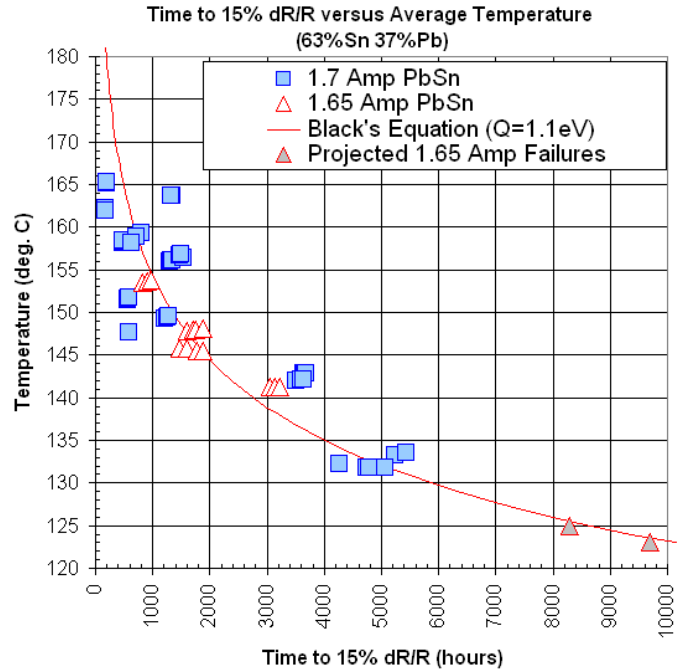

Figure 7 Plot showing the Time to Failure in eutectic SnPb solder bumps at 1.65A, 1.7A in addition to low temperature failure predictions.

RESISTANCE ANALYSIS

In these experiments, average resistance measurements on the large and small solder bumps were 26 mΩ and 30 mΩ, respectively. Quick estimates of the resistance due to the solder ball can be approximated by assuming a cylindrical shape for the solder ball. Using the dimensions shown in *Table 3*, and a Sn63Pb37, solder bump resistivity of ρ_{solder} = 146mΩ-μm, it can be seen that the actual impact of the solder ball on the total measured resistance is relatively small.

	Ball Diameter	Height	Via Dia.	Bump Res.	Measured Res.
Large Ball	285	240	250	0.55 mΩ	26 mΩ
Small Ball	237.5	185	210	0.48 mΩ	30 mΩ

Table 3 Calculated and average measured solder bump resistance.

The bulk of the measured resistance values must come from the Al interconnect traces on the test chip and PC board. In the large bump case, the daisy chain layout of the Cu and Al traces have equal XY lateral dimensions and via sizes. Thus the relative ratio of these two resistance sources can be estimated from the sheet resistance values shown in *Table 4*. Approximate resistance values and their contribution to the total measured resistance are shown in *Figure 8* and *Table 4*.

Material	Resistivity ρ(mΩ-μm)	Thickness t (μm)	Sheet Res. Rs(mΩ/sq.)	Large Bump-mΩ	Small Bump-mΩ
Test Chip-Al	38.41	0.835	46	25.2	29.3
UBM-Al	28	1	28	0.6	0.5
UBM-NiV	632	0.33	2110		
UBM-Cu	17	0.8	21.25		
Sn63Pb37	146	-	-		
PC Board-Cu	17	38.1	0.4462	0.2	0.2
			Total:	26	30

Table 4 Estimated resistances and their impact on the total experimentally measured resistance.

Cross-sections indicate that failure occurs only in solder bumps where the electron wind is directed away from the silicon die. In these solder bumps, failure occurs at the highlighted location, were Cu in the UBM is consumed during SnCu intermetallic formation, and material transport due to the electron wind results in vacancies pileup and voiding at the UBM/Solder interface. Vacancies move in the direction opposite to material transport and pileup at the Cu_6Sn_5 intermetallic where the bonding energy is high [6].

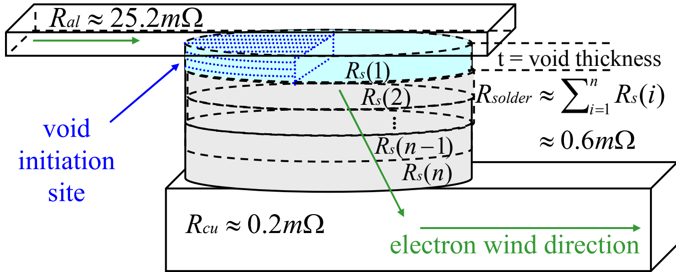

Figure 8 Schematic depiction of the sources of experimentally measured resistance (Large Bump Case).

As a rough estimate, the shape of the void can be assumed to be given by dimensions shown in *Figure 9*. Using this approximation, the fractional change in via area due to void growth can be calculated from:

Eq. (2)
$$\frac{dA}{A} = \frac{1}{\pi}\arccos\left(\frac{L}{r}\right) - \frac{1}{\pi}\left(\frac{L}{r}\right)\sqrt{1-\left(\frac{L}{r}\right)^2}$$

where A is the via area, dA is the void area, r is the via radius, V is the void length and L = r – V. In the no void case, L = r; for the 50% voiding case, L = r; and, in the 100% voiding case, L = -r.

As void progression occurs from left to right, the total change in resistance, dR_{total}, results from the resistance increase due to via closure, dR_{via}, and the resistance due to the added resistive path length above void, dR_{path}.

Eq. (3)
$$dR_{total} = dR_{via} + dR_{path}$$

The resistance increase due to via closure, dR_{via}, can be approximated by the equation:

Eq. (4)
$$dR_{via} = \frac{t\rho_{solder}}{\left(r^2\pi - dA\right)} - \frac{t\rho_{solder}}{r^2\pi}$$
$$= \frac{t\rho_{solder}}{r^2}\left(\left(\pi - \arccos\left(\frac{L}{r}\right) + \left(\frac{L}{r}\right)\sqrt{1-\left(\frac{L}{r}\right)^2}\right)^{-1} - \frac{1}{\pi}\right)$$

where t is the void thickness and ρ_{solder} is the resistivity of the solder.

As can be seen in *Figure 8*, the impact of via closure upon measured resistance is only important in the final stages of the solder bump lifetime. This is because the voided region, t, is only about 5 to 15 microns thick, so that even with 50% via closure, the dimensional change in the resulting semicircular cylindrical element, results in a resistance increase of only about 0.04 mΩ.

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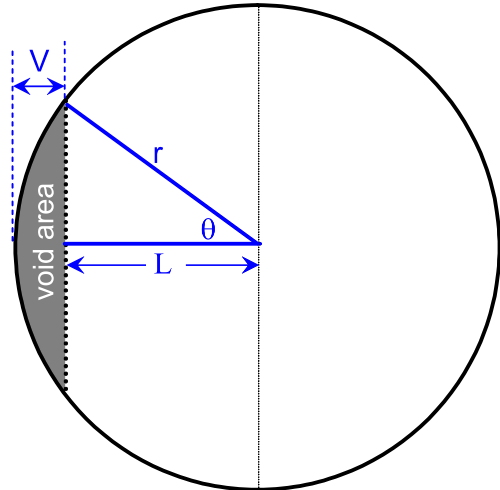

Figure 9 The relationship between via radius, r, and the void dimensions, V and L.

Assuming parallel current flow into the solder bump, a number of simplifying assumptions can be made when estimating resistance due to the added resistive path length. A simple geometric calculation of the number of squares, which can fit into the semicircle above the void has been shown to give a reasonable estimate of the electrically measured change in resistance [2]. This resistance can be calculated by multiplying "the geometric number of squares" by "the sheet resistance of the channel formed during via closure". Thus the resistance increase due to the added resistive path length, dR_{path}, can be approximated by the equation:

$$\text{Eq. (5)} \qquad dR_{path} = \tfrac{1}{2} R_{s-path} \left[\tfrac{\pi}{2} - \arcsin\left(L/r \right) \right]$$

where, $R_{s\text{-}path}$ is the sheet resistance of the newly created path length. In the current Al/NiV/Cu UBM, the upper bound in this estimated sheet resistance has been estimated to be ≤ 17 mΩ/sq [2].

Figure 10 shows that the change in resistance due to via closure, dR_{via}, is insignificant when compared to the effect of the added resistive path length above the void, dR_{path}. The small relative value dR_{via} results from the small quantity t/r^2 in Eq. (4). The major difference between the Eq. (4) and Eq. (5) can be thought of as being caused by the difference in resistance measurement direction in a thin metal disk with a pancake shape. The Y direction resistance through the central axis of a thin metal disc will be much lower than its X direction resistance along a lateral radial direction. As *Figure 10* shows, the resistance due to via closure only becomes significant when the via opening dimensions approach the size of the void thickness, t.

Thus Eq. (4) can be essentially ignored, and it can be shown that total change in resistance depends only upon the L/R ratio and $R_{s\text{-}path}$. Since via closure only depends upon the L/r ratio, Eq. (2), this means that the absolute change in resistance gives a direct measure of the fractional change in via opening dimensions independent of the bump diameter tested.

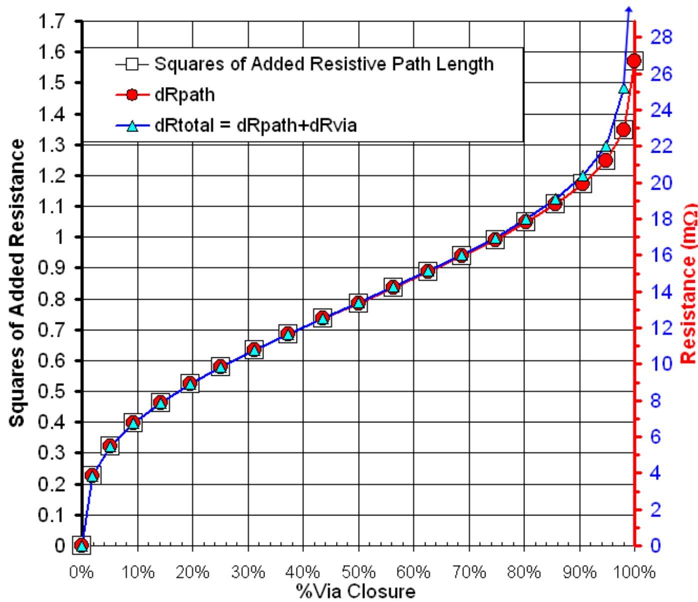

Figure 10 Graph showing the relationship between "via closure" and "squares of added resistive path length". Also shown are "the bump resistance due to path length only" and "the total change in bump resistance".

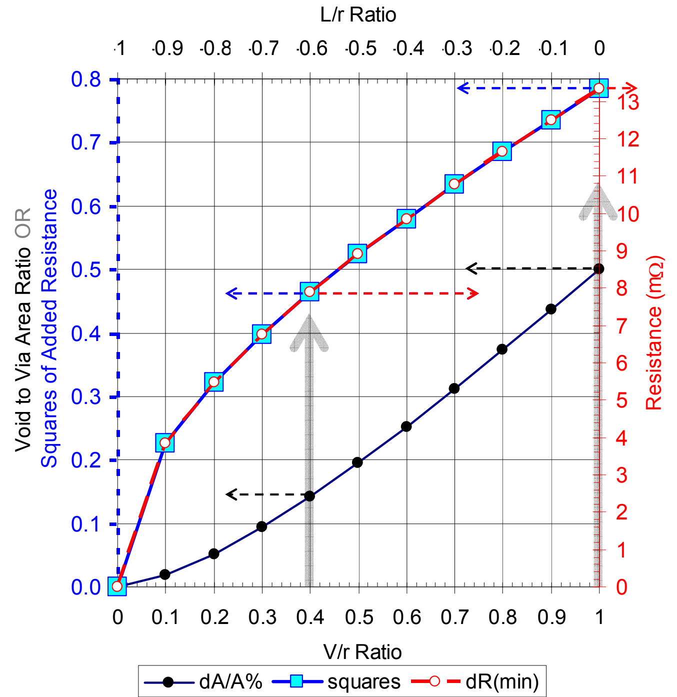

Figure 11 Graph showing the relationships between the L/r and V/r ratios and 1) the Void to Via Area Ratio, 2) the number of squares of lateral void area, and 3) the change in bump resistance (for $R_{s\text{-}path}$ = 17 mΩ/sq).

For failure due to voiding in the solder/UBM interface, it becomes apparent that absolute change in resistance is a better gauge of failure progression than dR/R. In a daisy chain layout, division by R modifies the data by interconnect resistances, which are dependent upon test chip and circuit board layout. Thus, an absolute change in resistance should allow for better comparison between independent lab sites, since it is less dependent upon board and test chip layout, is independent of bump or via diameter, and can be more directly tied to the geometry of failure.

Figure 10 and *Figure 11* show the graphical relationships between dA/A and the estimated change in resistance using Eq. (2) and Eq. (5). As can be seen in these figures, when void length equals via radius (V/r=1), the void to via area ratio equals 0.5, which corresponds to 0.79 squares of added resistive path length. Using an assumed sheet resistance of 17 mΩ/sq, results in a 13.4 mΩ expected change in bump resistance.

In the large bump case, the 15% dR/R failure criterion corresponds to a 3.9 mΩ change in average bump resistance. Since voiding only occurs in half of the solder bumps, the actual change in the voided bumps is closer to 7.8 mΩ. As is shown in *Figure 11*, this corresponds to a V/r ratio of about 0.4 or a percentage via closure of about 15% or about 0.46 squares of added resistive path length.

DISCUSSION

Based upon the source resistance analysis in the previous section, the conversion of the numerous %dR/R data files collected over the last year was initiated. *Figure 12* shows one section of typical ongoing testing, after this conversion to absolute change in resistance. The chart shows room temperature testing, done inside of an enclosed and vented oven, in order to avoid problems in case of thermal runaway. The X axis is scaled in 24 hr increments in order to show the effect of ambient temperature upon the test results. The sinusoidal resistance and temperature curves result from the lab air conditioning being turned on in the mornings and shut-off during the evenings, i.e., during the summer, heating occurs at night and cooling during the days.

During the temperature calibration of these boards, the temperature coefficient of resistance of the wide daisy chain interconnect traces was not collected. However, *Figure 12* indicates that the temperature compensation for these traces should also be considered. *Figure 13* shows temperature compensation, using the dR/dT values from neighboring temperature sensors on the same die. The two days where morning cooling is absent, correspond to the weekend, when air conditioning is not needed. The required dR/dT temperature compensation values calculated from the temperature sensor resistors was 0.31% Ω/ °C (3100 ppm/°C). If not accounted for, this indicates that a 50°C increase in die surface temperature would result in a resistance change comparable to the 15% dR/R failure criteria. Thus, temperature compensation in the interconnect traces should result in a reduced spread in the MTTF curves shown in *Figure 4* and *Figure 7*.

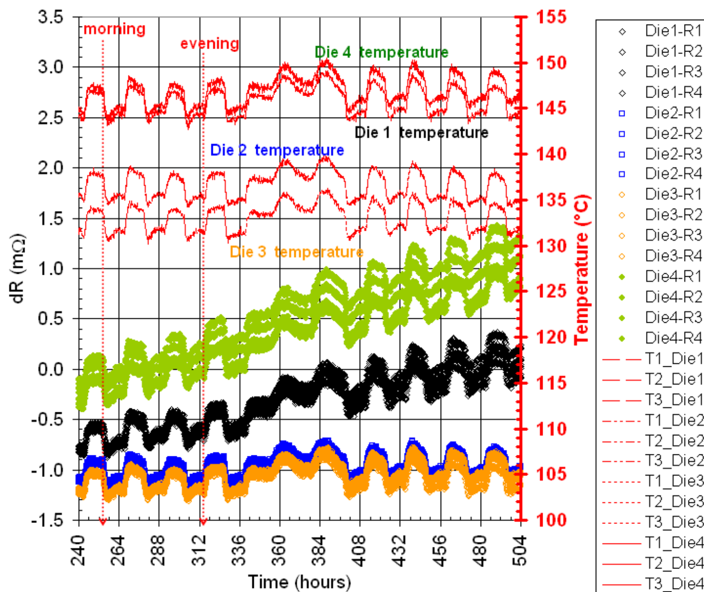

Figure 12 Absolute bump resistance and temperature measurements (1.7 A, lead-free, Small Bump).

Figure 14 shows testing on a lead-free small bump PC Board, in which testing was done at three different temperatures using a current of 1.7 A. One the first day (Friday), a fully loaded oven (12 boards) set a 50°C, showed thermal runaway in the ambient temperatures measured by the oven temperature controller. The testing was shut down over the weekend and restarted on the following Monday with the oven shut off. Testing was halted 4 days later (Friday), to adjust the Nitrogen flow into the oven, in order to allow for lower oven ambient temperatures. Failure occurred 2 weeks later, on a weekend, when rising solder bump resistances, resulted in runaway die surface temperatures. Testing was stopped prior to exceeding the melting point of the no Pb solder (217°C). Testing was resumed on Die 2 and Die 3 after jumper wiring across the failed die. The data just prior to the week of Die 1 and Die 4 failure is shown in *Figure 15*.

In the small bump case, 15% dR/R corresponds to a 4.5 mΩ change in average bump resistance. Since only solder bumps with currents directed into the die experience voiding, this corresponds to a resistance of change of 9 mΩ or a 20% reduction in estimated void opening dimensions. Since thermal runaway can be attributed to Joule heating to Eq. (5), it should in theory be possible to improve electromigration reliability by increasing the Al layer thickness in the Al/NiV/Cu UBM system.

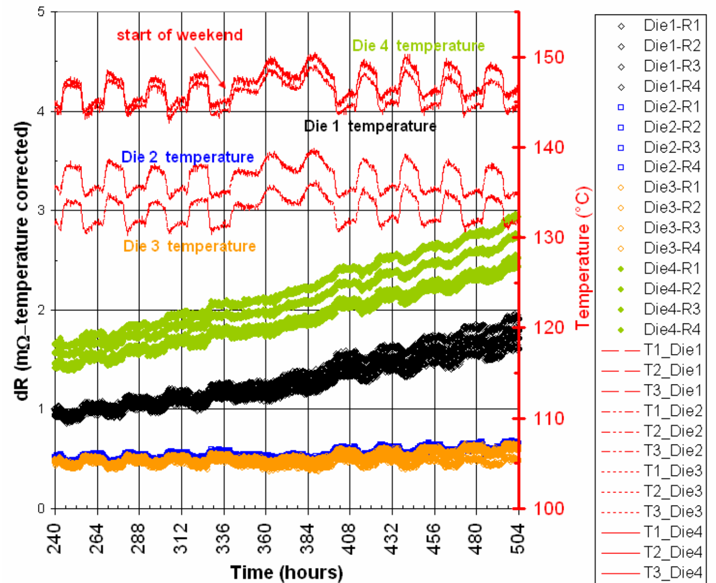

Figure 13 Temperature compensated bump resistance measurements (1.7 A, lead-free, Small Bump).

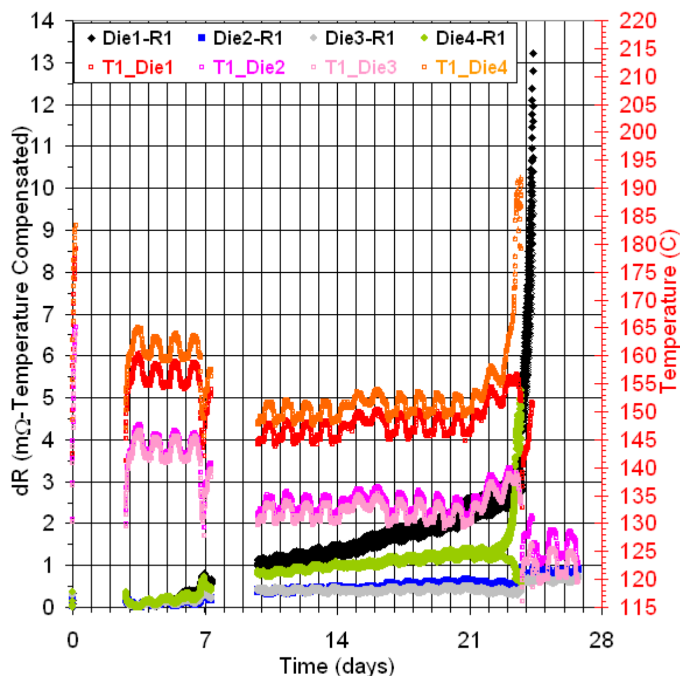

Figure 14 Temperature compensated bump resistance measurements showing weekend failure on two hotter running die, Board #Vb12 (1.7 A, lead-free, Small Bump).

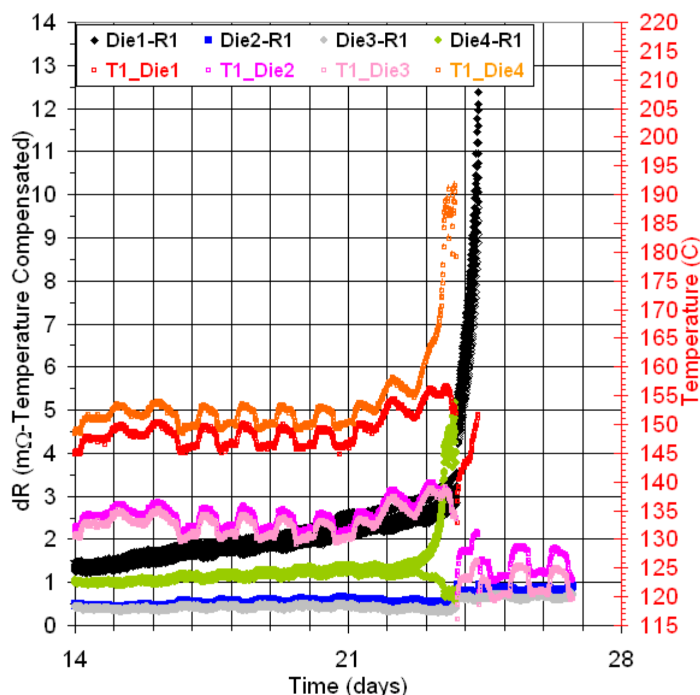

Figure 15 The week just prior to Die 1 and Die 4 failure on Board #Vb12 (1.7 A, lead-free, Small Bump).

FUTURE WORK

Alternatively, even smaller diode temperature sensors could be employed. In order to maintain isothermal heating conditions for a better fit to Black's Equation, the temperature sensor can also be used as a heater, to maintain a fixed temperature through computer controlled, Joule, self heating, i.e., as the temperature in the solder bump rises due void growth, the current through the temperature sensor can be adjusted to maintain isothermal heating conditions.

The additional metal layer could also be used to add multiple voltage sense nodes along the expected pathway for voiding. This would give a simple real-time indication of the void growth, allowing direct comparison with calculated and measured change in resistance. This layout methodology would also bypass interconnect resistances, eliminating the need for interconnect temperature compensation and improve measurement precision by at least a factor of 25. *Figure 16* shows how such a layout might be accomplished.

CONCLUSIONS

Using 4-point Kelvin resistance measurement techniques and an automated test system with high density switching matrix, activation energies due to electromigration-induced voiding are determined in eutectic SnPb and no Pb solders (SAC405). At the temperature and current densities examined, the activation energy for eutectic SnP was 1.1 eV. This indicates that the driving mechanism for material transport and reverse vacancy migration is lattice diffusion. For SAC 405, the measured activation energy was 0.84 eV, indicating interfacial material transport as the dominant transport mechanism.

Based upon a proposed analytical model for calculating resistance changes due to solder bump voiding, procedures for how to quantify electromigration damage are presented. For "pancake type" voiding at the UBM/solder interface, it has been determined that the measured change in resistance should give a direct indication of the percentage change in bump via opening dimensions, independent of solder bump diameter.

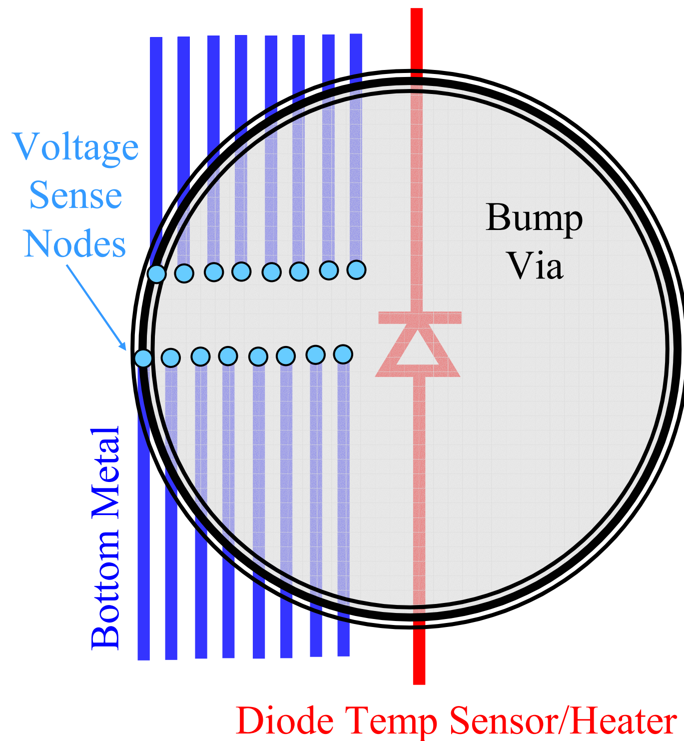

Figure 16 Proposed layout for critical analysis of the void growth in an individual solder bump.

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