A Structured Approach To Lead-Free IC Assembly Transitioning

L. Nguyen, R. Walberg, Z. Lin, T. Koh*, YY Bong**, MC Chua**, S. Chuah**, JJ Yeoh***
National Semiconductor Corp.
P.O. Box 58090 M/S 19-100
Santa Clara, CA 95052-8090

* *National Semiconductor, Singapore*
** *National Semiconductor, Melaka, Malaysia*

Abstract

Market forces, trade restrictions, and customer perceptions rather than environmental realities have driven the lead-free movement. However, it cannot be turned around. Consequently, manufacturers, suppliers, and industry consortia have all been working towards a common acceptable drop-in replacement for the standard eutectic SnPb. Most U.S. and European groups support the use of SnAgCu alloys for surface mount applications. For instance, NEMI has recommended Sn3.9Ag0.6Cu as an industry standard for lead-free solder paste (with Sn0.7Cu for wave soldering), and is currently assessing its manufacturability and reliability. Similarly, SnAgCu alloys have been recommended for solder balls to be used in array packages. Unfortunately, there has been no recommendation for a lead-free finish for leaded packages, which still constitute the largest portion of the worldwide semiconductor packaging production. IC suppliers had to struggle to evaluate the various lead-free finish options available, and assess the resulting impact of the transition on their manufacturing logistics.

This paper will provide the highlights of a structured program at National Semiconductor Corp. to transition from SnPb to lead-free IC manufacturing.

Introduction

Initiatives to reduce the release of lead into the environment gained momentum in the 1990s, with legislation being proposed in various countries to restrict, tax, and even outlaw lead. For the electronics industry, this triggered a search for a drop-in alternative to the tin-lead (SnPb) solder used in electronic assemblies, namely, printed wiring board coatings, solder paste, and component finishes. A number of recent conferences and symposia have been devoted exclusively to the topic of lead-free manufacturing [1,2].

Major challenges facing the transition to lead-free include:

1. High temperature compatibility with up to 260°C reflow temperature required for non-optimized processes, and up to 245°C with new equipment and optimized processes.
2. MSL degradation of plastic packages.
3. Risk potential for passive devices and connector/socket body materials.
4. Forward/backward compatibility (reliability, quality, rework, and dual inventory).
5. Lack of test standards for reliability issues (e.g., whiskering).
6. Supply chain readiness (materials and equipment suppliers).
7. Weak push/pull for lead-free parts.

Although demand in the U.S. and Europe is still low, requests from key strategic partners in Japan have prompted National Semiconductor to develop a structured program to transition to lead-free IC packaging. This program was organized as a three-phase process.

- *Phase 1* addressed the Moisture Sensitivity Level (MSL) reclassification of existing packages for 260°C reflow temperature.
- *Phase 2* evaluated the lead-free finish options for leaded packages. The manufacturing evaluation included plating studies, package reliability testing, board assembly investigation, board level reliability testing, subcontractors' qualification, and logistics assessment. Matte Sn was selected as the finish offered for all the leadframe-based packages, and SnAgCu was the solder ball alloy for substrate-based array packages. SnAgCu was also selected and qualified for the micro SMD – NSC's Wafer Level-Chip Scale Packages [3].
- *Phase 3* extends the MSL performance of packages affected in *Phase 1* by the MSL downgrade due to the higher reflow temperature. Materials sets (e.g., die attach, mold compounds, and substrates) that enhanced the MSL performance are being evaluated. *Phase 3* is scheduled to be completed for NSC's package portfolio by the end of CY 2002.

The structured approach allowed for a timely and smooth transition from the standard SnPb semiconductor manufacturing to the anticipated lead-free IC demand.

Reflow Profiles

Phase 1 of the project consisted of reclassifying all surface mount packages using the lead-free reflow profile. The packages had already been classified according to the standard IPC/JEDEC profiles defined in J-STD-020A, with the peak reflow temperature dependent on the package body size (see *Table 1*). The standard reflow profiles, as defined in J-STD-020A, are given in *Table 2*.

For reclassification at the lead-free reflow temperatures, the NEMI proposal was adopted (see *Table 3*). This lead-free reflow profile was used regardless of the package body size. *Figure 1* compares the standard 220°C profile with the lead-free profile.

MSL Reclassification Methodology

The reclassification of National's packages using the 260°C profile was accomplished using the following approach:

1. Package selection:
    a. Each package body size (or each body width in the case of dual inline packages) within each package family was represented.
    b. For the given package body size, the largest die attach pad size was chosen.
2. Preliminary moisture/reflow evaluations were done using the 260°C profile. The standard MSL and the next lower (more sensitive) MSL were used. The damage response (cracking/delamination) was assessed using an acoustic microscope. If the package failed both levels based on IPC/JEDEC J-STD-020, then the next lower MSL was evaluated.
3. Based on the preliminary results, either one or two MSL's were selected for the following reliability evaluations, which were done on two assembly lots per package type:
    a. Preconditioning + Autoclave (96 hours) – 50 parts/lot.
    b. Preconditioning + TMCL (500 cycles, -65°C to +150°C, 2 cycles/hour) – 77 parts/lot.

MSL Reclassification Results

Representative reclassification results are shown in *Table 4*. Basic properties of the mold compounds used in these packages are shown in *Table 5*. The following observations were made:

1. The mini packages (SOT-23 and MSOP) remained at Level 1, including both low stress ECN and biphenyl mold compounds.
2. The standard mold compound, C, did not fare very well at 260°C on the SOIC packages. In the case of the 8L SOIC, this was due to die surface delamination at Level 2A.
3. The TO-252 with the low stress compound passed Level 2 at 260°C, exhibiting die surface delamination at Level 1.
4. The 100L TQFP maintained MSL Level 2 at 260°C, whereas the 100L LQFP dropped from Level 2A to Level 3. Although they are both built with the same biphenyl mold compound, the TQFP has a significantly smaller die attach pad, leading to a more robust package.
5. The 100L PQFP, with the improved moisture performance ECN, was found to pass Level 3 at 260°C, failing Level 2A due to popcorn cracking.

The PBGA and EBGA packages were found to fail the minimum Level 4 requirement at 260°C. Recently, however, new mold compounds and die attach materials have been found that improve the MSL of these packages to Level 3 at 260°C, with no changes required for the organic substrates. These materials are now being qualified as part of *Phase 3*.

Lead-Free Lead Finish Selection and Qualification

Phase 2 of the project consisted of selecting and qualifying a lead-free lead finish. The following steps were taken:

1. Characterization of candidate plating materials.
2. Selection of final candidate(s).
3. Characterization of lead-free plating line.
4. Package level qualification.
5. Board level qualification.

Characterization of Candidate Plating Materials

The following plating materials were characterized: Sn, SnCu, SnAg, and SnBi. NiPd, as a lead finish was qualified several years earlier, and was also included in the overall evaluation matrix.

Characterization was done on leadframes made of two different copper alloys: C7025 and C194. The evaluation consisted of:

1. Visual inspection: appearance and whiskers.
2. Cracking or flaking after trim and form.
3. Solderability after 16 hours steam aging.
4. Wetting time.

With the exception of whiskers on the C194 with SnCu plating, all of the plating materials performed acceptably on both copper alloys. It is to be noted that these whiskers were formed during plating (rather than as a result of a stress-relieving mechanism subsequent to plating), and resulted from a non-optimized plating bath.

Selection of Final Candidate(s)

A decision tree was created to rank order the various lead-free alloy candidates. The key factors considered included: manufacturability, materials availability, costs (equipment and materials), board assembly, reliability, customer acceptance, subcontractors' readiness, and timing.

A number of factors quickly narrowed the previous list of candidates for plating. Pre-plated SnAg leadframes were available from selected suppliers. However, at the time of the investigation, SnAg was not available yet as a commercial plating solution from key suppliers, and the timeframe for its introduction was still questionable. SnBi suffers from slow plating throughput and bath stability compared to the conventional SnPb plating line, and has limited acceptability in Japan. The same concerns that had restricted the wide use of NiPd as a lead-free finish in the early 1980s have not vanished, namely, different finished appearance compared to SnPb affecting inspection equipment, high cost of the precious metal combined with limited raw material sources, and long-term political instability of the geographical locations of such sources (Russia and South Africa). Some independent results also pointed out the dependency of the assembly yield of NiPd packages on the soldering process [4].

Characterization of Lead-Free Plating Line

As a result, it was decided to drop SnAg, SnBi, and NiPd from further consideration. Thus, plating lines were set up to evaluate only both Sn and SnCu plating chemistries. Again, characterization was done on both C7025 and C194 leadframes. The results were as follows:

__Sn__

- Same efficiency as SnPb plating line.
- Meets plating thickness requirement.
- No whiskers observed.
- High current density showed no problems.
- Bath remained stable after 9 days storage.
- All parts passed solderability test.

__SnCu__

- Estimated composition: 2.0% Cu.
- Plating efficiency 30% lower than SnPb.
- Frame oxidation observed with current stoppage.
- Foaming occurred in plating cell and tank.

Based on the above results, it was decided to primarily focus on Sn plating for the subsequent efforts.

Package Level Qualification

The purpose of the package level qualification was to assess the effect of the Sn plating on solderability, lead plating integrity, whisker growth and package reliability.

For the preconditioning of the parts prior to package reliability tests, the lead-free reflow profile was used with the MSL as determined in the previous phase of the project. The whisker growth was measured at each time point of the THBT tests using an optical microscope at 40X. A failure was considered to be the presence of any whisker greater than or equal to 2 mils. The solderability test consisted of steam aging the parts for 16 hours at 100^{o}C, followed by dipping the leads into the solder bath. The criterion was at least 95% solder coverage.

The following is a summary of the qualification:

Packages:
20L SOIC WIDE
9L TO-263
48L TSSOP
176L LQFP

Reliability Tests:
TMCL (-65/150^{o}C), 1000 cycles, s/s = 77
THBT, 1000 hours, s/s = 77
HTSL, 1000 hours, s/s = 77
ACLV, 96 hours, s/s = 77

Other Tests:
Solderability.
Checking of solder cracks before and after trim and form.
Measure whiskers after THBT time points.

All packages passed the above qualification.

Additional Evaluations

In addition to the above qualification, a series of tests were done to satisfy the requirements of a particular customer. These tests included the following:

1. Whisker growth after 500 cycles TMCL followed by 85^{o}C/85% RH for 500 hours.
2. Solderability using a wetting balance with solder paste.
3. Terminal robustness, measuring the force required to break the solder joint between the package lead and the PCB land area.

The packages that were evaluated included the SOT-23 and the TO-252. Upon examination at both 40X and at 300X magnification, there was no evidence of any whisker growth for either package.

Table 6 shows the results of the wetting balance. The results indicated that SnPb parts with SnPb solder paste have better wettability (shorter wetting time) than either the Sn or the SnPb lead finish with the SnAgCu paste. In addition, due to the greater lead surface area, the TO-252 exhibited greater wetting times than the SOT-23.

For the terminal robustness test, the parts were preconditioned for 4 hours in an autoclave (121^{o}C, 100% RH) prior to surface mount. The PCB's were designed with land patterns according to the IPC standards for the given package. The boards were designed with perforations between the land patterns such that after board mount, each mounted package could be singulated to enable attaching the punched out PCB section to the mounting jig on the Instron tester. The mounting jig was designed to hold the PCB section at a 45^{o} angle. An 8-mil wire was threaded through a single lead and then clamped to a small fixture affixed with a hook to the Instron load cell. The measured pull strength values, both before and after TMCL, are given in *Table 7*. The data showed that the Sn finish with SnAgCu paste resulted in significantly stronger solder joints than does SnPb finish with SnPb solder paste. In addition, it is noted that TMCL (1000 cycles of –35/+105^{o}C) did not affect the solder joint strength for either SnPb or lead-free.

Board Level Qualification

The selection of packages for the board level qualification was based on the following criteria:

1. Include all lead configurations (gull wing, J-bend, and land contact area).
2. Represent a wide range of package body sizes.

The above criteria were decided upon because these factors have the greatest influence on the stress that the solder joint experiences during board level temperature cycling. *Table 8* shows the selected packages.

Due to cost considerations, each PCB was designed to accommodate all package types on each of two sides. Thus, only a single PCB layout was needed. The board material was FR4 of thickness 1.6 mm. Two types of board surface finishes were evaluated: electroless nickel-immersion gold (NiAu) and organic solder preservative (OSP).

Prior to the board assembly process, evaluations were performed in order to determine the most appropriate reflow profile to use for each of the two solder pastes. First of all, blank PCB's were printed with SnPb and Sn3.5Ag0.7Cu pastes. Both standard and linear profiles were run. The standard profiles had a leveling out of the thermal gradient in the preheat region, whereas the linear profiles had a near-constant slope throughout the thermal ramp. The peak temperature for both types of profiles was 230°C for the SnPb paste and 240°C for the lead-free paste. The results showed no visible difference in wetting between the standard and the linear profiles for either solder paste. The difference seen was between the NiAu PCB's and the OSP PCB's, where the NiAu board finish was seen to result in better solder paste wetting than the OSP.

Additionally, daisy-chained parts representing all three lead finishes were mounted to the PCB's using both the standard and the linear profiles and both solder pastes. The electrical resistance data showed no difference between lead finishes, solder pastes or profile types. Lead pull tests were performed on the 208L PQFP, which also showed no statistical difference between lead finishes, solder pastes or profile types. Cross sections of the 56L LLP showed that the solder joint was void-free for the standard profile, whereas the solder joint from the linear profile exhibited voiding. Thus, the standard profile was chosen for the assembly builds.

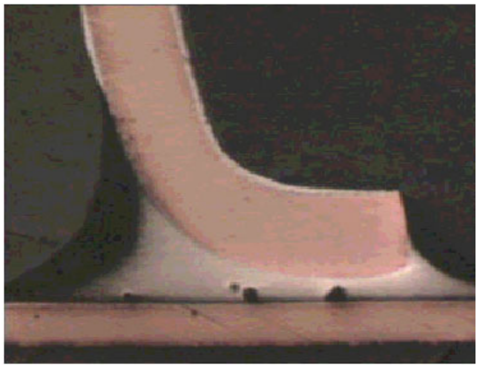

Figure 2: *208L PQFP solder joint (Sn leadfinish; SnAgCu solder paste with NiAu PCB surface finish).*

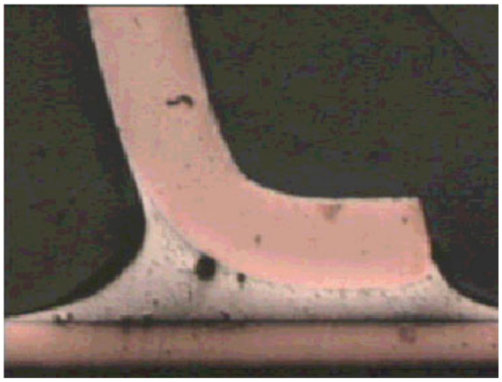

Figure 3: *208L PQFP solder joint (SnPb lead finish; SnPb solder paste with NiAu PCB surface finish).*

The board level qualification was done using daisy-chained parts on boards that were monitored for electrical continuity throughout the course of temperature cycling. In addition, the drop and vibration tests were done only on the LLP packages. Three lead finishes were evaluated: Sn, SnCu, and SnPb. For each of the three lead finishes, two solder pastes were used: Sn3.5Ag0.7Cu and SnPb. All combinations and numbers of good parts undergoing the tests are shown in *Table 9*. The test results are shown in *Table 10*. *Figures 2* and *3* compare the cross sections of the lead-free PQFP with SnPb PQFP, respectively. There is no noticeable difference in the solder joint appearance.

The only failures were seen on the 56L LLP. After numerous cross-sections were examined and the PCB design was reviewed, it was determined that the LLP failures were not due to the lead-free solder paste or lead finishes, but were related to the PCB design. Retesting of the 56L LLP is currently underway using an improved PCB design, which will result in better solder joints and better board level reliability results.

Implementation Logistics

There were several considerations relating to the implementation of lead-free lead finish. First of all, to handle the transition, it was decided to offer lead-free parts on an as-requested basis. The small initial lead-free volumes would then be managed by using subcontractor plating lines. The internal plating lines would be converted after the lead-free volumes became significant.

Early in the program, prior to lead-free lead finish qualification, customer requests were received for standard SnPb parts for reflow on lead-free boards at 260°C. In order to accommodate both these requests and lead-free lead finish requests, it was decided to offer two new process flows as follows:

1. The "**260C**" flow that would allow for standard SnPb parts to be packed for reflow at 260°C. Thus, a PQFP package, requested with the "260C" flow, would be shipped at Level 3 rather than Level 2A.
2. The "**NOPB**" flow that would allow for lead-free parts to be shipped at the appropriate MSL.

Another key consideration in the lead-free implementation was the marking of parts. For simplicity, it was decided to leave the part name unchanged. At the same time, it was realized that traceability was necessary. Several marking options were discussed, including (1) the adding of an additional character immediately before the part name; (2) adding a slash (/) immediately after the date code; (3) using lowercase letters; (4) beginning the die run code with the letters R – Z. Options (1) and (2) were eliminated due to the fact that many of the parts were not physically able to accommodate any additional characters. Option (3) was eliminated due to the fact that the ordering system was not able to distinguish between upper and lowercase letters. Thus, option (4) was chosen since it could be easily applied without any major changes to the system. The only modification that was made was to have the backend systems automatically assign a die run code beginning with the letters R – Z to those parts that had been flagged as lead-free.

Conclusions

The company-wide effort to transition from standard SnPb to lead-free packaging has successfully completed the first two phases, namely the MSL reclassification, and the offering of lead-free packages independent of MSL. *Phase 1* showed that the higher temperature reflow could degrade the MSL of certain packages. In *Phase 2*, matte Sn was chosen as the lead-free finish for leadframe-based packages, while SnAgCu was selected for the solder balls in array packages. *Phase 3*, the offering of lead-free packages with enhanced MSL performance is ongoing at the time of this writing. *Phase 3* is scheduled to be completed for all the packages in NSC's packaging portfolio by the end of CY02.

Acknowledgments

The lead-free initiative (which also includes halogen-free packaging) involves a number of groups within different organizations at National Semiconductor Corp. The authors would like to thank the following individuals: M. Kim and A. Khan (Quality and Reliability); M. Hepp, T. James, and J. Williams (Customer Quality Engineering); J. Anderson and S. Gutierrez (Planning); R. Hung and A. Hui (Purchasing); A. Beyrich and M. Schnepf (NSC, Germany); A. Yoshimoto, K. Mita, and S. Gohara (NSC, Japan).

References

1. *IPC Works 1999*, October 23-28, 1999, Minneapolis, MN; *IPC Works 2000*, September 9-14, 2000, Miami, FL; *IPC/JEDEC Int. Conf. On Lead-Free: Electronic Components and Assemblies*, May 1-2, 2002, San Jose, CA.
2. "Lead-Free – Fantasy or Fact", *MEPTEC 2000*, June 14, 2000, Sunnyvale, CA; "Summit on Lead-Free Solder Implementation," *MEPTEC 2001*, January 10, 2001, San Jose, CA; "Lead-Free Solder Implementation Summit," *MEPTEC 2001*, August 30, 2001, Sunnyvale, CA.
3. Patwardhan, V., Nguyen, L., and Kelkar, N., "Lead-Free Wafer Level Chip Scale Package: Assembly and Reliability," *52nd Electron. Comp. & Tech. Conf.,* May 28-31, San Diego, CA (2002).
4. Hunt, C., "An Assessment of Lead-Free Palladium-Finished Components: The Impact on Assembly Yields with Conventional Tin/Lead Solder," *Proc. IPC Works 2000*, p. S-02-2, Miami, FL (2000).

***Table 1**: Standard Peak Reflow Temperatures from IPC/JEDEC J-STD-020A.*

<table>
<tr><td>Pkg. Thickness ≥ 2.5 mm and all BGAs</td><td>Pkg. Thickness < 2.5 mm and Pkg. Volume ≥ 350 mm^3</td><td>Pkg. Thickness < 2.5 mm and Pkg. Volume < 350 mm^3</td></tr>
<tr><td colspan="2">Convection 220 +5/-0°C</td><td>Convection 235 +5/-0°C</td></tr>
</table>

***Table 2**: Standard Reflow Profiles from J-STD-020A.*

Average ramp-up rate (183°C to Peak)	3°C/second max.
Preheat temperature 125°C (± 25°C)	120 seconds max.
Temperature maintained above 183°C	60-150 seconds
Time within 5°C of actual peak temperature	10-20 seconds
Peak temperature range	220 +5/-0 °C or 235 +5/-0 °C
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	6 minutes max.

***Table 3**: Pb-free Reflow Profile.*

Average ramp-up rate (217°C to Peak)	3°C/second max.
Preheat temperature 150°C (± 25°C)	60-120 seconds
Temperature maintained above 217°C	60-150 seconds
Time within 5°C of actual peak temperature	10-20 seconds
Peak temperature	260 (-5/+0) °C
Ramp-down rate	6°C/second max.
Time 50°C to peak temperature	3.5 minutes min., 6 minutes max.

***Figure 1**: Reflow Profiles.*

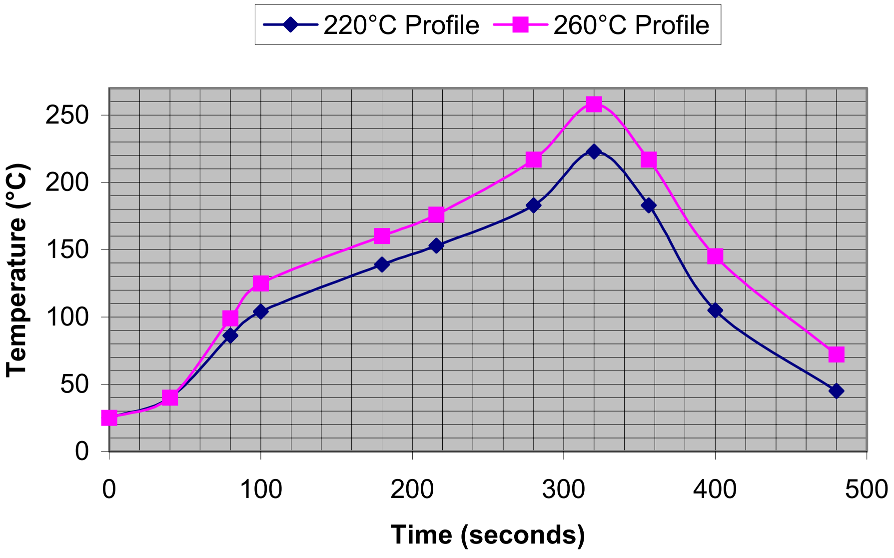

Table 4: *MSL Reclassification Results.*

Lead count/ Package	**Body Size (mm)**	**Mold Compound**	**Die attach pad size (mm)**	**Standard Reflow**		**MSL at 260°C**
				Peak Temperature (°C)	**MSL**	
6L SOT-23	1.6x2.92x1.02	A	0.89x1.5	235	1	1
8L MSOP	3x3x0.86	B	1.7x2.4	235	1	1
8L SOIC	3.9x4.9x1.45	C	2.2x3.0	235	1	3
20L SOIC	7.5x12.8x2.34	C	4.8x6.1	220	1	2A
3L TO-252	6.6x7.3x2.3	A	3.2x4.3	235	1	2
100L TQFP	14x14x1.0	B	5.5x5.5	235	2	2
100L LQFP	14x14x1.4	B	7.6x7.6	235	2A	3
100L PQFP	14x20x2.7	D	9.1x9.1	220	2A	3

Table 5: *Mold Compound Properties.*

Mold Compound	***A***	***B***	***C***	***D***
Description	Low Stress	Best moisture performance	Standard	Improved moisture performance
Epoxy Type	ECN	Biphenyl	ECN	ECN
Filler Loading (%)	76	85	72	81
Tg (°C)	155	135	155	150
α_1 (cm/cm-°C)	14×10^{-6}	10×10^{-6}	20×10^{-6}	11×10^{-6}
α_2 (cm/cm-°C)	55×10^{-6}	42×10^{-6}	56×10^{-6}	47×10^{-6}
Flexural Modulus (kg/mm^2)	1110	2300	1550	2100
Moisture Absorption (24 hour boiling, %)	0.30	0.17	0.30	0.22

Table 6: *Results of the Wetting Balance.*

Package	**Lead Finish**	**Solder Paste**	**Avg. Wetting Time (sec)**	**Max. Wetting Time (sec)**	**Min. Wetting Time (sec)**
SOT-23	Sn	SnAgCu	1.99	2.39	1.69
	SnPb	SnAgCu	1.96	2.24	1.76
	SnPb	SnPb	0.71	0.94	0.46
TO-252	Sn	SnAgCu	5.34	6.41	4.75
	SnPb	SnAgCu	3.58	4.00	3.20
	SnPb	SnPb	3.46	4.10	3.03

Table 7: *Results of the Terminal Robustness Test.*

Package	**Lead Finish**	**Solder Paste**	**Avg. Pull Force before TMCL (Newtons)**	**Avg. Pull Force after TMCL* (Newtons)**
SOT-23	Sn	SnAgCu	15.9	14.2
	SnPb	SnPb	9.4	10.1
TO-252	Sn	SnAgCu	51.7	51.5
	SnPb	SnPb	25.2	31.8

**TMCL: 1000 cycles of –35/105°C*

***Table 8**: Packages Selected for Board Level Qualification.*

Package	Body Size (mm)	Lead Configuration
208L PQFP	28 x 28 x 3.4	Gull Wing
84L PLCC	29 x 29 x 3.7	J-Bend
20L PLCC	8.9 x 8.9 x 3.7	J-Bend
9L TO-263	10.2 x 8.7 x 4.6	Gull Wing
5L SC-70	1.25 x 2.0 x 0.9	Gull Wing
56L LLP	9 x 9 x 0.75	Land Contact
8L LLP	2.5 x 2.5 x 0.75	Land Contact

***Table 9**: Evaluation Legs and Sample Sizes for Board Level Qualification.*

Package	Test	Sn3.5Ag0.7Cu Paste			Sn3.5Ag0.7Cu Paste			SnPb Paste			SnPb Paste		
		NiAu			OSP			NiAu			OSP		
		Sn	SnCu	SnPb	Sn	SnCu	SnPb	Sn	SnCu	SnPb	Sn	SnCu	SnPb
PQPF 208L	TMCL	32	32	34	32	32	32	32	32	32	32	32	32
PLCC 84L	TMCL	32	32	31	32	32	32	32	32	32	33	32	33
PLCC 20L	TMCL	80	80	82	82	81	81	81	80	81	81	81	81
TO-263 9L	TMCL	80	80	80	80	80	80	80	80	80	80	80	80
SC-70 5L	TMCL	80	80	80	80	80	80	80	80	80	80	80	80
LLP 56L	TMCL	82	80	81	80	81	80	82	82	80	78	80	80
LLP 8L	TMCL	80	80	80	80	80	80	80	80	80	80	78	80
LLP 56L	Drop	24	19	23	24	21	24	22	17	24	24	15	24
LLP 8L	Drop	22	22	22	22	22	22	22	22	22	22	22	22
LLP 56L	Vib.	22	21	24	24	24	23	23	23	24	21	22	23
LLP 8L	Vib.	22	22	22	22	22	22	22	22	22	22	22	22

***Table 10**: Board-Level Failures.*

Package	Test	Sn3.5Ag0.7Cu Paste			Sn3.5Ag0.7Cu Paste			SnPb Paste			SnPb Paste		
		NiAu			OSP			NiAu			OSP		
		Sn	SnCu	SnPb	Sn	SnCu	SnPb	Sn	SnCu	SnPb	Sn	SnCu	SnPb
PQPF 208L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
PLCC 84L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
PLCC 20L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
TO-263 9L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
SC-70 5L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
LLP 8L	TMCL	0	0	0	0	0	0	0	0	0	0	0	0
LLP 8L	Drop	0	0	0	0	0	0	0	0	0	0	0	0
LLP 56L	Vib.	0	0	1	0	0	0	0	0	2	0	3	6
LLP 8L	Vib.	0	0	0	0	0	0	0	0	0	0	0	0