Effect of current crowding on void propagation at the interface between intermetallic compound and solder in flip chip solder joints

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We propose a kinetic model to describe a pancake-type void propagation in flip chip solder joints due to current crowding in electromigration. The divergence of the vacancy fluxes at the interface between the solder and Cu_6Sn_5 leads to void formation and propagation along the interface between them. Based on the continuity condition, the void growth velocity is calculated. The theoretical calculations are in reasonable agreement with the experimental results. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2158702]

The trend in miniaturization and the pursuit of greater performance in microelectronics industry have led to a significant increase of current density in packaging technology.[1,2] The average current density in flip chip solder joints has reached 10^4 A/cm^2, consequently electromigration has become a reliability issue in electronic packaging.[3–7] Due to the line-to-bump geometry in a flip chip configuration and high homologous temperature, the electromigation behavior and mechanism of void formation in solder joints are quite different from that in Al or Cu interconnects.[8–10] It is uniquely dominated by current crowding at the cathode contact of a solder bump where a very large change of current density occurs. The typical failure mode is the propagation of a pancake-type of void across the cathode contact interface. When the void eclipses the entire contact, an abrupt and dramatic increase of resistance of the circuit is detected, indicating circuit failure. So far, no modeling of the current crowding induced void formation has been reported. A kinetic model of the void propagation is presented in this letter.

Experimentally, eutectic SnPb flip chip solder joints were stressed by current density of 2.55×10^4 A/cm^2 at 150 °C.[6] After 38 h, voids started to form at the interface between the intermetallic compound (IMC) and solder, but it only took 5 h for the pancake-type voids to propagate across the whole interface, resulting in an open circuit failure. Also, the electromigration reliability behavior of a daisy chain of 20 flip chip solder joints of both eutectic SnPn and Pb-free (95.5Sn–4.0Ag–0.5Cu) solder bumps with Al/Ni(V)/Cu thin film underbump metallization was tested at current density of 3.67×10^3 A/cm^2 and the bump temperature was at 146 °C.[7] After a 15% increase of resistance, the cross section of a set of bumps in the daisy chain was examined. Figure 1 is the scanning electron microscopy (SEM) image of the cross section of the cathode contact of a solder bump where a pancake-type void formation at the interface between IMC and solder is seen. In the daisy chain, the void has been observed at alternate bumps at the cathode contact where the current enters the bump from the Al interconnect line.[7]

Figure 2 shows a two-dimensional simulation of current distribution in the flip chip solder joint shown in Fig. 1. The current density at the entrance corner is approximately one order of magnitude higher than the average current density in the bump, which is defined as the current crowding region. During electromigration, atoms in the solder bump will be driven to the anode due to the high current density, and a corresponding vacancy flux comes back to the cathode interface. Because of the large bonding energy or formation energy of vacancies in Cu_6Sn_5, the flux of vacancy entering the IMC is small. Therefore, a flux divergence of vacancy occurs at the interface, which will lead to vacancy supersaturation, in turn nucleation and condensation of void formation at the interface. The void will grow since it is the sink of ensuing vacancies supplied by electromigration. As the void grows, it displaces the current crowding region to the growth front of the void. Based on this physical picture, we develop a model to describe the kinetics of void propagation at the interface between the IMC and the solder.

In Fig. 3, the curved lines represent the electron flow direction. The solid arrow lines depict the flux from Cu_6Sn_5 to the solder where the current crowding pushes the atom from the top to the bottom. Meanwhile, the vacancies go back from the solder to Cu_6Sn_5 with the dotted arrow line.

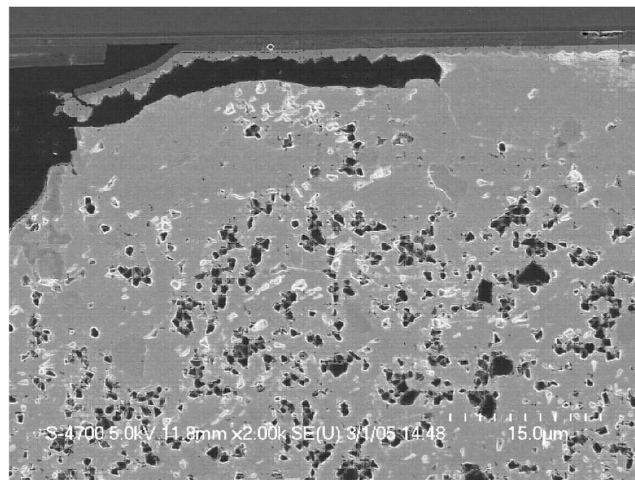

FIG. 1. SEM image of void formation in flip chip 95.5Sn–4.0Ag–0.5Cu solder bump.

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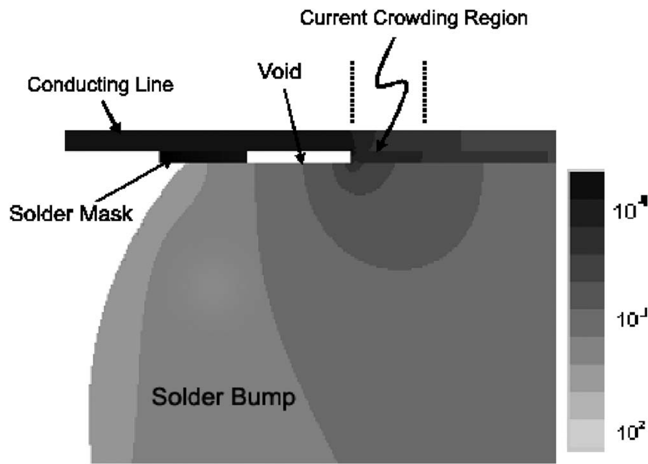

FIG. 2. Two-dimensional simulation of current distribution in the solder bump. A schematic diagram depicts the current crowding region.

The electron wind effect and the corresponding vacancy fluxes in the Cu_6Sn_5 and solder are written as, respectively,

$$J_{\eta}^{\nu} = \frac{C_{\eta}^{\text{bulk}} D_{\eta}}{kT} Z_{\eta}^{*} e \rho_{\eta} j,$$

$$J_{\text{Sn}}^{\nu} = \frac{C_{\text{Sn}}^{\text{bulk}} D_{\text{Sn}}}{kT} Z_{\text{Sn}}^{*} e \rho_{\text{Sn}} j, \tag{1}$$

where J_{η}^{ν} is the vacancy flux of Cu_6Sn_5 and J_{Sn}^{ν} is the vacancy flux insider the solder. D is the diffusivity, e is the charge of an electron, ρ is resistivity, and j is current density. Z^* is the effective charge number of electromigration, which includes the electrical field effect and the momentum exchange effect.

The solder/IMC interface provides the transport path for excess vacancies and enables them to diffuse along the interface. The lateral flux due to the divergence of vacancies can be written as

$$J_{\text{int}}^{\nu} = -D_{\text{int}} \frac{\Delta C}{\Delta x} \approx D_{\text{int}} \frac{\Delta C}{b'}, \tag{2}$$

where D_{int} is the diffusivity in the interface, b' stands for the width of current crowding region, and ΔC is the concentration difference between the concentration in the higher current density and the equilibrium concentration at the tip or growth front of the void. In terms of mass conservation law, we have

$$J_{\text{int}}^{\nu} a \delta = (J_{\text{Sn}}^{\nu} - J_{\eta}^{\nu}) a b', \tag{3}$$

where δ is the effective thickness of interface and a is the width of interface.

It is assumed that the thickness of void is d, and J_{void} is the flux of vacancy at the tip of the void. The continuity equation of flux is applied again

$$J_{\text{int}}^{\nu} a \delta = J_{\text{void}} a d. \tag{4}$$

Substituting Eq. (3) and (4), the flux to grow the void can be written as

$$J_{\text{void}} = (J_{\text{Sn}}^{\nu} - J_{\eta}^{\nu}) \frac{b'}{d}. \tag{5}$$

On the other hand, we can give the volume of matter transported by J_{void} along the interface

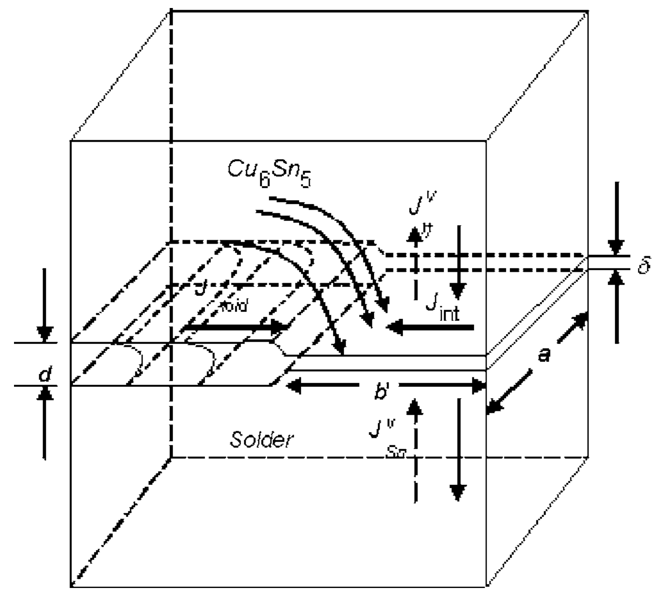

FIG. 3. Schematic illustration of the void propagation along the interface between solder and IMC. The curved lines stand for the electron flow direction. δ is the thickness of interface, d is the width of void formation, b' is the width of current crowding region, and a is the width of interface.

$$\Delta V = J_{\text{void}} A \Delta t \Omega, \tag{6}$$

where $\Delta V = a d \Delta l, A = a\delta$, and Ω is the atomic volume.

Inserting Eq. (5) into (6), the growth velocity of void becomes

$$\nu = \frac{\Delta l}{\Delta t} = (J_{\text{Sn}}^{\nu} - J_{\eta}^{\nu}) \frac{b'}{d} \Omega. \tag{7}$$

We know $C_{\nu}^{\text{bulk}} \Omega = 1$ and obtain

$$\nu = \frac{ej}{kT} (D_{\text{Sn}} \rho_{\text{Sn}} Z_{\text{Sn}}^{*} - D_{\eta} \rho_{\eta} Z_{\eta}^{*}) \frac{b'}{d}. \tag{8}$$

In order to verify the mechanism of void propagation, we should pay attention to two key parameters; one is the width of current crowding region, b', and the other is the width of the void, d. As shown in Fig. 3, Gibbs-Thomson effect[11] may play an important role in forming the tip of the void

$$C_r = C_0 \exp\left(\frac{2\gamma}{r} \frac{\Omega}{kT} \right), \tag{9}$$

where γ is the surface energy per area and Ω is the atomic volume.

The linear approximation is adopted, and the void width can be written as

$$d = 2r = \frac{C_0}{\Delta C} \frac{4\gamma\Omega}{kT}. \tag{10}$$

Since our model is a two-dimensional model, the void width is assumed to be kept constant. On the other hand, we start from Eqs. (2) and (3), and can obtain the width of current crowding as

$$b' = \left[\frac{\Delta C}{C_0} \frac{kT D_{\text{gb}} \delta}{ej(D_{\text{Sn}} Z_{\text{Sn}}^{*} \rho_{\text{Sn}} - D_{\eta} Z_{\eta}^{*} \rho_{\eta})} \right]^{1/2}. \tag{11}$$

In our simulation shown as Fig. 2, the contact window length of eutectic SnAgCu solder joint is set to 250 μm as

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TABLE I. Theoretical and experimental values of current crowding width, void width and void growth velocity for eutectic SnAgCu.

	Theory	Experiment
b'	25.49–44.15 μm	37.5 μm
d	0.81–2.42 μm	2.44 μm
ν	1.24–6.44 μm/h	4.4 μm/h

the based diameter of the solder joint, and the current crowding region is about 15% of the whole length, so the current crowding region, b', is estimated to be about 37.5 μm. From Fig. 1, the void width, d, is measured as 2.44 μm. As shown in Fig. 1, the test temperature is 146 °C, the electric current density is about 3.67×10^3 A/cm^2, the void length is 26.4 μm, the void propagation has spent about 6 h, therefore the void growth velocity is about 4.4 μm/h.

The diffusivity is $D_{Sn}=1.3\times10^{-10}$ cm^2/s for Sn, $D_\eta=2.76\times10^{-13}$ cm^2/s for Cu_6Sn_5, and the diffusivity of interface is taken to be 4.2×10^{-5} cm^2/s.[12,13] The effective charge is $Z^*_{Sn}=17$ for Sn and $Z^*_\eta=50$ for Cu_6Sn_5.[14–16] The resistivity of Sn is $\rho_{Sn}=13.25$ $\mu\Omega$ cm and that of Cu_6Sn_5 is $\rho_\eta=17.5$ $\mu\Omega$ cm.[12] The surface energy per area $\gamma=10^{15}$ eV/cm^2 and Ω is taken as 2.0×10^{-23} cm^3.[12–16] The effective interfacial width is about 0.5 nm. The only unknown parameter is the ratio of ΔC and C_0. At 125 °C, it is reasonable to choose the range of $\Delta C/C_0$ from 1% to 3%.

Using these parameters and experimental conditions, we calculate the theoretical values of current crowding width b' from Eq. (11), void width d from Eq. (10), and void growth velocity ν from Eq. (8). The comparison between theoretical values and experimental results are in reasonable agreement as listed in Table I.

Electromigration induced void formation and propagation in Al interconnects has been studied and the effect of stress on slid-type void growth has been emphasized.[8–10] Comparing to Al, solder is a low melting alloy but its application occurs at a much higher homologous temperature, therefore thermally activated process dominants the event in solder joints even when mechanical stress might exist. The accumulation of non-equilibrium vacancies at the cathode should generate a tensile stress. In Eq. (9), the Gibbs-Thomson effect has addressed it implicitly. Thus, in our analysis, we focus on the diffusional process in electromigration driven by the current crowding effect and propose a kinetic model to describe the void propagation in flip chip solder joints. The stress effects are ignored but should be considered in the future.

In summary, the failure mode of electromigration in the eutectic SnPb and SnAgCu flip chip solder joints occurs by a pancake-type void formation and propagation at the interface between the solder and Cu_6Sn_5. The divergence of the vacancy fluxes at the interface leads to void formation and propagation along the interface. Based on the continuity condition, the void growth velocity is calculated. The theoretical calculations are in reasonable agreement with the experimental results.

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