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Simulated Power Cycling for Rapid Reliability Assessment of Pb-Free Packages

K. Setty¹, G. Subbarayan¹, L. Nguyen², D. Love³ and R. Sullivan⁴

¹School of Mechanical Engineering, Purdue University, West Lafayette, IN 47907, USA

²National Semiconductor Corporation, Santa Clara, CA, 95052, USA

³Sun Microsystems, Palo Alto, CA, 94303-4900, USA

⁴High Density Packaging Users Group, Scottsdale, AZ, 85253, USA

ABSTRACT

The Simulated Power Cycling (SPC) Test is a simplified powercycling test procedure since it does not need a die with a heater but instead uses an external thermoelectric device to heat the package surface. In this paper, we describe a tester design, its capabilities and the results of testing on a wafer-level Chip Scale Package (CSP). Through localized heating, the thermoelectric device enables rapid cycling of packages unlike in thermal chambers. The cycle time for accelerated testing of Pb-free solders is currently an industry concern since the rate of damage accumulation due to thermomechanical loading in Pb-free solders is different from the eutectic Sn-Pb solders. The tests were performed on a 36 I/O wafer scale CSP package.

Keywords: thermal fatigue testing, powercycling.

INTRODUCTION

Soldering is extensively used to assemble electronic components to printed circuit boards or chips to substrates in microelectronic devices. Solder joints serve as mechanical, thermal and electrical interconnections, therefore, solder joint integrity is a key reliability concern. Eutectic Sn37wt%-Pb solder, with a melting temperature of 183 C, is one of the most common solder alloys due to its high strength and resistance to creep. However, there are mounting health and environmental concerns about the toxicity of Pb present in these alloys and the search for potential replacement alloys has been an area of extensive research in recent years [1-4]. One of the solutions proposed by many researchers is to use Sn based alloys with silver and/or copper being the other alloying elements. At present there is a shortage of data on the mechanical behavior of these alloys as appropriate to the service conditions. Plumbridge et al. demonstrated that the mechanical properties of the lead-free alloys may be better or worse than those of the eutectic Sn-Pb alloys depending on the test conditions [5-6]. As

a practical matter the reliability of the new lead free alloy candidate must be compared with the eutectic Sn-Pb alloy to assess the reliability of the Pb-free solders over the full range of today's electronic industry applications.

The use of accelerated tests to characterize the reliability of electronic packages is well established at the present time in the microelectronics industry. The widely used accelerated life test at the present time is the accelerated temperature cycle (ATC) test where the components or printed circuit assemblies are placed inside a chamber, which is cycled between the extremes of temperature. During this cycling, at each instant, the oven operates quasi-statically, reaching a uniform temperature instantaneously (Figure 1).

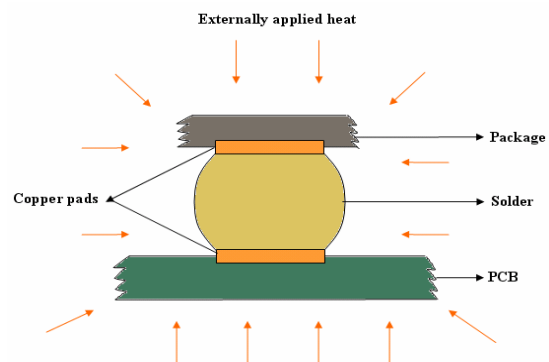


Figure 1: Schematic of externally applied heat during an ATC test in an environmental chamber.

The popularity of the thermal cycling test is at least in part owed to the simplicity of concept and of operation. However, in recent years, there is a growing debate on the validity of thermal cycling tests since under the field use conditions, where the heat is generated by a powered electronic device and

as a result the package is under anisothermal conditions. Thus, it is believed that power cycling accelerated test (PCT), in which the package is differentially heated (Figure 2), is more representative of the field use conditions and that no one test is preferred from a failure mechanism point of view [7]. One advantage of power cycling test (PCT) is that the typical cycle is nearly an order of magnitude shorter than the typical thermal cycling test. This will enable quick reliability assessment and help in reducing development time and cost.

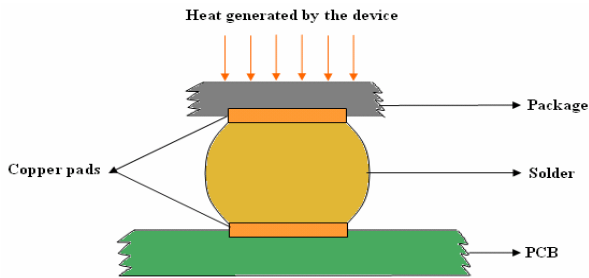


Figure 2: Schematic of heat generated/applied during PCT/SPC Test.

In the present paper we describe the design of a new SPC tester, its capabilities and some typical results from the tests performed on four NSC 36 I/O wafer scale CSP packages using this tester.

SPC TESTER DESIGN

Overall a significant amount of effort was required to debug the tester to eliminate the noise in the system. In this paper emphasis is placed on the final tester design.

The Objectives of the SPC tester were to provide test instrumentation capable of loading the package in a manner more representative of field use conditions, controlling ramp rates and dwell times (within a tolerance of $\pm 2.5^{\circ}\text{C}$), accommodating a temperature range of upto 130°C , accommodating electronic components ranging in size from 0.25 to 2.0 in² and reducing the overall time required for accelerated thermal life tests on micro-electronic components.

Figure 3 shows the schematic of the designed SPC tester. It consists of two distinct parts, the electrical system and the cooling system.

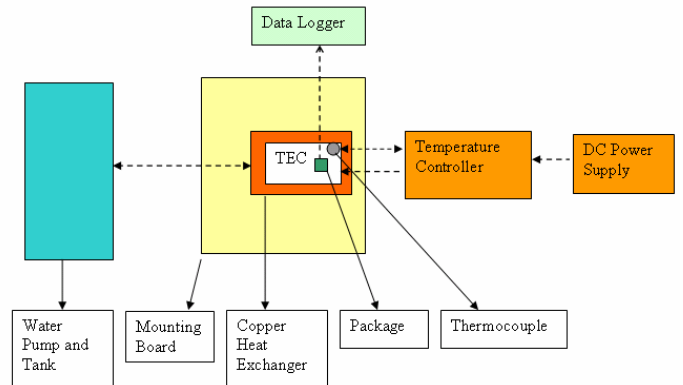


Figure 3: Schematic of the SPC tester

Electrical System

The electrical system consists of a DC power supply, a temperature controller, peltier devices and thermocouples. A peltier or a Thermoelectric cooler (TEC) is a solid-state device that operates as a heat pump. It consists of p and n type semiconductors which act as thermoelectric cooling couples which are electrically in series and thermally in parallel, therefore heat absorbed at the cold junction is pumped to the hot junction at a rate proportional to the current passing through the circuit and the number of couples. The surface near the hot junction becomes hot while the surface near the cold junction becomes cold. The hot surface is used to heat up the package surface and thereby the solder. When the direction of the current is reversed, the direction of heat transport is reversed. Therefore, using a peltier device, a thermal cycle consisting of ramps to high or low temperatures and dwell times at these temperatures can be achieved. To facilitate thermal fatigue cycling, a T-type thermocouple was used on the peltier surface for temperature feedback to a temperature controller through an interface program capable of fatigue cycling.

Cooling System

The cooling system consists of an immersible water pump, a copper heat exchanger and a water tank. The water pump was used for circulating water through a copper heat exchanger which facilitates faster ramp down and maintains the dwell time profile during testing. Running water as opposed to recirculated water was used to maintain a consistent temperature profile during successive thermal cycles. Alternative designs using a water chiller with an adequate water flow rate and cooling capacity are also possible.

CAPABILITY

Ramp rates of 2°C/s were achieved and various temperature profiles were consistently maintained throughout the testing process. Also, field use conditions are simulated due to differential heating in the package. Therefore a thermal cycle which is nearly an order of magnitude shorter than and more representative of field use condition than the typical thermal

cycling test can be achieved. Electronic components in the size ranges of 0.25 to 2 in² can be tested. The above described SPC tester is capable of testing 32 packages at a time. However, this is not a limitation of the design since more components can be tested by simply adding more controllers.

TEST VEHICLE AND MOUNTING

A 65-mm x 50-mm FR4 card with four 36 I/O wafer scale CSP package packages attached on it was used for this study (Figure 5). The solders in all the packages were daisy chained and wires were soldered to the terminals in each package for continuous resistance monitoring. A data logger was used for monitoring the resistance in all the packages. The four packages on a FR4 card were mounted upside down on the peltier device and thermally cycled between 0 and 100 °C.

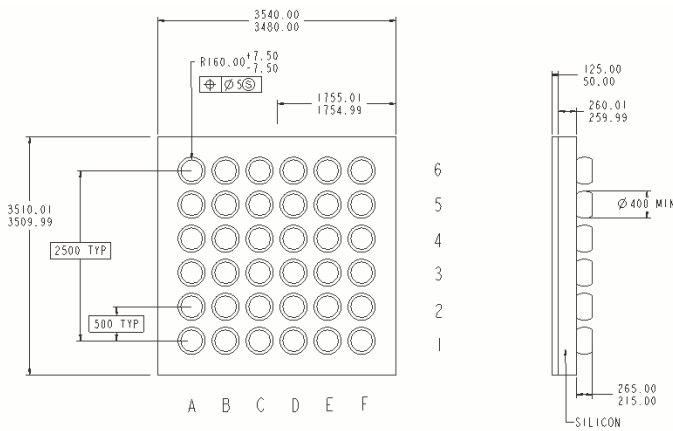


Figure 5: Schematic of the NSC 36 I/O wafer scale CSP package

SPC THERMAL PROFILE

Bartelo et.al [8] conducted experiments to compare the fatigue life of SAC and eutectic solders at temperature ranges of 0 to 100⁰ C and -40 to 125⁰ C. They found the fatigue life SAC solders to be better than the eutectic solders in the 0 to 100⁰ C temperature range. However, in the -40 to 125⁰ C range, the eutectic solders were found to have a better fatigue life. With further experiments they found that the cold dwell temperature has little effect on the relative fatigue life. It was concluded that the change in the fatigue life was due to either hot dwell peak temperature or due to the differences in the strain range imposed by the respective temperature ranges or due to both

It is widely known in the micro-electronic industry that most of the damage accumulation in a solder occurs during the hot dwell. For the purposes of accelerated testing it is desirable to allow the solders to relax “sufficiently” at hot dwell. Shortening the dwell time in an accelerated test leads to less fatigue damage per cycle and a relatively longer fatigue life. On the other hand a longer dwell time results in an almost complete creep/stress relaxation during the hot dwell in each

cycle and consequently a relatively shorter fatigue life. Further, in references [8, 9] it was observed that the increase in the hold/dwell time dramatically reduces the number of cycles to failure for solder and leads to a saturation in cycles to failure. Therefore it is crucial to allow just “sufficient” relaxation in the solders during test conditions so that we can accurately relate the life under test conditions to the life in the majority of the field use conditions. To understand the effect of dwell times on the fatigue life of SAC solders Sahasrabuddhe et.al [9] conducted thermal shock tests. They found that the fatigue life was most sensitive to hot dwell times in the range of 5 to 10 minutes and beyond the 10 minute hot dwell time the dependence of fatigue life on hot dwell time was found to be insignificant. In our experiments we assume a similar dwell time dependence of fatigue life for SAC solders and choose a thermal profile with a 7 minute hot dwell. It is also widely believed that the ramp times have a relatively insignificant effect on the fatigue life [10, 11]; therefore the thermal profile (Figure 4) details of our experiments are shown in table 1.

SPC TEMPERATURE MONITORING

Temperature on the peltier surface was monitored for temperature feedback purposes. Under the given testing conditions, a simple one-dimensional calculation shows that the temperature drop in the silicon die of thickness 200 microns and area 3.5mm X 3.5mm is about 2.9 °C. Given that the temperature variation during the hot dwell is about +2 °C, temperature monitoring at the peltier surface is within reasonable tolerances.

| Profile Metric | Profile Metric Value |
|-------------------|----------------------|
| Hot dwell time | 7 minutes |
| Cold dwell time | 1 minute |
| Cycle time | 10 minutes |
| Peak Temperature | 100 °C |
| Temperature Range | 100 °C |

Table 1. Thermal Profile Metric

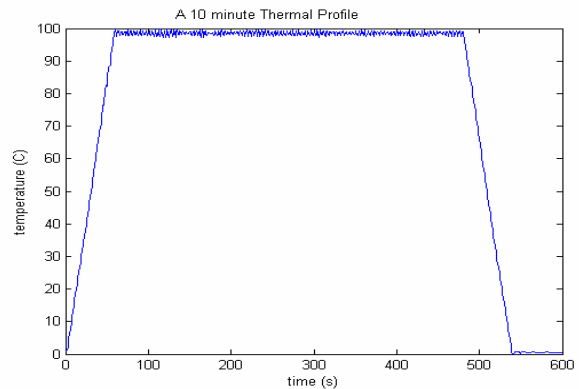


Figure 4: A 10 minute Thermal profile used for SPCT

FAILURE CRITERIA

A consistent resistance variation of 3-4 ohms was observed in the daisy chained solder area array throughout the duration of the test prior to failure. A 250% increase in the resistance from the normal value (10 ohms) was chosen as a failure criterion.

RESULTS

The results of testing four 36 I/O WLCSP packages with the SPC tester are shown in Table 2.

| Package | Life |
|---------|------|
| 1 | 2730 |
| 2 | 2750 |
| 3 | 2800 |
| 4 | 3196 |

Table 2: Package life under power cycling test conditions

CONCLUDING REMARKS

A unique SPC tester was built and optimized for minimal temperature fluctuation. Its capabilities were discussed. 4 NSC 36 I/O wafer scale CSP were tested under powercycling conditions using the SPC tester. Consistent results in terms of fatigue life were obtained in all cases. These results in terms of the fatigue life of packages show promise for future widespread use of the SPC tester as a primary thermal fatigue tester for electronic packages experiencing differential heating. Most importantly the SPC tester will enable quick reliability assessment and help in reducing the development time and cost.

ACKNOWLEDGMENTS

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