



*New Family of Integrated  
Buck Regulators using  
Emulated Current Mode (ECM)*

**Presented by: Bob Bell  
Application Engineer  
Phoenix, AZ**

1

Welcome to National Semiconductor's continuing series of on-line webcasts.

My name is Bob Bell, I'm an application engineer from Phoenix Arizona.

Today's topic is an introduction to a family of Integrated Buck Regulators using a new form of control that we refer to as Emulated Current Mode control.



## *Webcast Outline*

---

- **Buck Regulator Basics**
- **Operation of Current Mode Control**
- **Operation of Emulated Current Mode Control**
- **New Family of Simple Switcher Regulators**
- **Thermal Considerations**
- **Loop Compensation Design**
- **Inverting Buck-Boost Application**

The topics I plan to cover in this presentation are:

Buck Regulator Basics

Operation of Current Mode Control

Operation of Emulated Current Mode Control

New Family of Simple Switcher Regulators

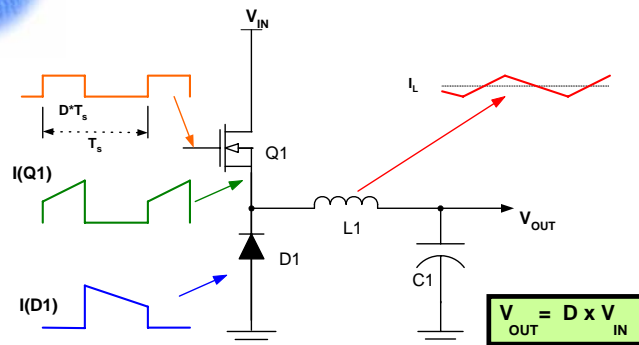
Thermal Considerations

Loop Compensation Design

Inverting Buck-Boost Application



## Buck Regulator Waveforms and Characteristics



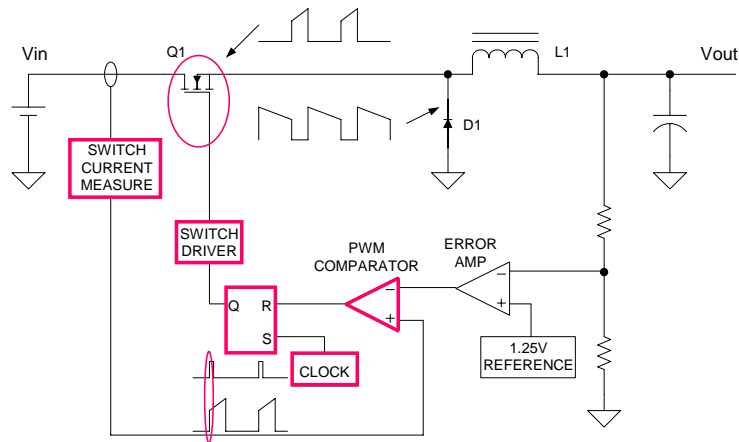
- Non-Isolated Grounds
- Voltage Step-down Only
- Single Output Only
- Very High Efficiency
- Low Output Ripple Current
- High Input Ripple Current
- High Side (Floating) Gate Drive Required
- Large Achievable Duty Cycle Range
- Wide Regulation Range (due to above)

Shown on this slide is the power stage for a step-down buck regulator. The output voltage is stepped down by modulating the duty cycle of the MOSFET, Q1. When the MOSFET turns on  $V_{in}$  is applied to the LC output filter. The transfer function of this regulator is  $V_{out} = D \times V_{in}$ , where  $D$  is the duty cycle of the modulating switch, Q1. The diode D1 provides a path for the inductor current to flow when Q1 is turned off.

Each cycle the inductor current ramps up while Q1 is on and then ramps down while the diode is conducting. The MOSFET and diode currents sum to form the inductor current. The current waveforms are shown.



## Buck Regulator with Current Mode Control



Shown on this slide is the same basic buck regulator power stage with the addition of the control circuitry. Control is accomplished through pulse width modulation of Q1. This particular control circuit is referred to current mode control. The main characteristic of current mode control is that the modulating ramp used by the PWM comparator is a signal derived from the buck switch current. When the buck switch is turned on, the current rises with the same profile as the inductor current.

Each period the modulation of Q1 is controlled as follows:

It can be seen that there are quite a few steps that need to be accomplished each period. The minimum time required to complete these steps creates a minimum controllable on-time or duty cycle. For large step-down applications with a large  $V_{in}$  and much smaller  $V_{out}$  this minimum on-time can present a problem. The biggest challenge when designing for minimum on-time is the design of the current measure circuit. We'll talk more about this in the following slides.



## *Current Mode Control Advantages / Disadvantages*

### ADVANTAGES

- Current mode control is a single pole system. The current loop forces the inductor to act as constant current source.
- Current mode control remains a single pole system regardless of conduction mode (continuous mode or discontinuous).
- Inherent line feed-forward since the ramp slope is set by the line voltage.
- By clamping the error signal, peak current limiting can be implemented.
- Ability to current share multiple power converters.

### DISADVANTAGES

- Susceptibility to noise on the current signal is a very common problem, reducing the ability to process small on-times (large step-down ratios).
- As the duty cycle approaches 50% current mode control exhibits sub-harmonic oscillations. A fixed slope ramp signal (slope compensation) is generally added to the current ramp signal.

The objective of this presentation is not to cover every detail of current mode control, but I would like to list the main advantages and disadvantages associated with current mode control.

#### ADVANTAGES:

- Current mode control is a single pole system. The current loop forces the inductor to act as constant current source.
- Current mode control remains a single pole system regardless of conduction mode (continuous mode or discontinuous).
- Inherent line feed-forward since the ramp slope is set by the line voltage.
- By clamping the error signal, peak current limiting can be implemented.
- Ability to current share multiple power converters.

#### DISADVANTAGES:

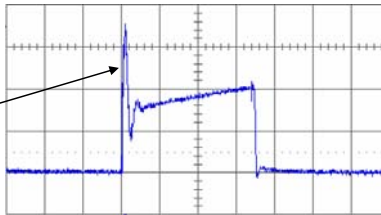
- Susceptibility to noise on the current signal is a very common problem, reducing the ability to process small on-times (large step-down ratios).
- As the duty cycle approaches 50% current mode control exhibits sub-harmonic oscillations. A fixed slope ramp signal (slope compensation) is generally added to the current ramp signal.
- The advantages for current mode control are compelling. The objective of this presentation is to present a solution for the noise susceptibility problem that has been plaguing designers since the discovery of current mode control.

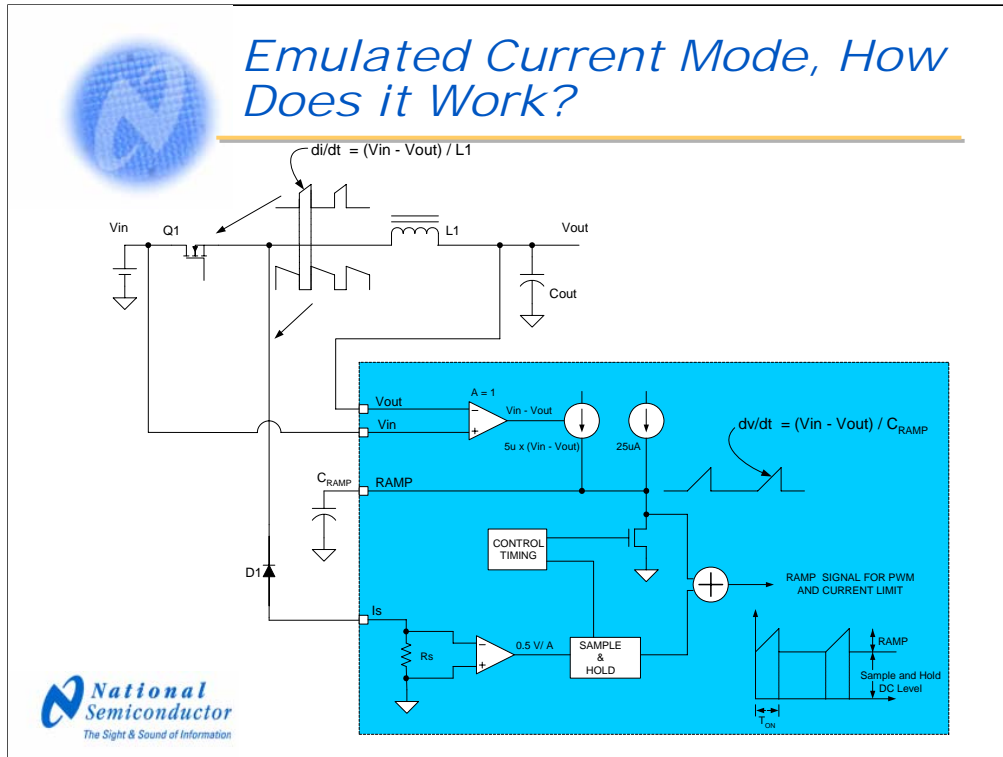


## Why Emulated Current Mode?

- Step down switching regulators designed for high input voltages must control very short minimum on-times to operate at high frequencies.
- The maximum switching frequency (and size of the inductor and output capacitor) are function of the minimum on-time.
- The on-time of conventional current mode controllers is limited by current measurement delays and the leading edge spike on the current sense signal. When the Buck FET turns on and the diode turns off, a large reverse recovery current flows, this current can trip the PWM comparator. Additional filtering and / or leading edge blanking is necessary to prevent premature tripping of the PWM. The emulated current signal is free of noise and turn-on spikes.

Leading edge spike,  
conventional current  
mode control.





Shown of this slide is the buck regulator power stage comprised of Q1, D1, L1 and Cout.

The objective is to create a signal that accurately represents the current through the buck switch Q1 without actually making a direct measurement.

When we study the characteristics of the buck switch current signal we can note that the signal can be broken down into two parts, a pedestal and a ramp. When the buck switch initially turns on the current level jumps to the same level that was conducting previously in the diode. By taking a sample-and-hold measurement of the diode current just before turning on the buck switch we can establish the pedestal level. A small current sense resistor is placed in series with the diode anode to accomplish this measurement.

Once the buck switch is turned on the characteristic of the ramping current is:

$$di/dt = (V_{in} - V_{out}) / L \quad \text{This is the basic inductor equation.}$$

To emulate the ramping portion of the buck switch signal first we create a current source proportional to the difference between the input and the output voltage. If this current source flows into a capacitor, the ramping voltage across the capacitor will equal:

$$dv/dt = (V_{in} - V_{out}) / C$$

If we set the value of the capacitor proportional to the inductor value we can scale the capacitor voltage to match the ramping current signal.

The final step is to add the sample and hold diode current level to the capacitor ramp voltage. Now we have recreated the buck switch signal with no delays and no leading edge noise spike. We can now use this signal for pulse-width modulation and current limit purposes as in conventional CM control. Each period after the buck switch turns off the ramp capacitor is discharged in preparation for the next cycle.

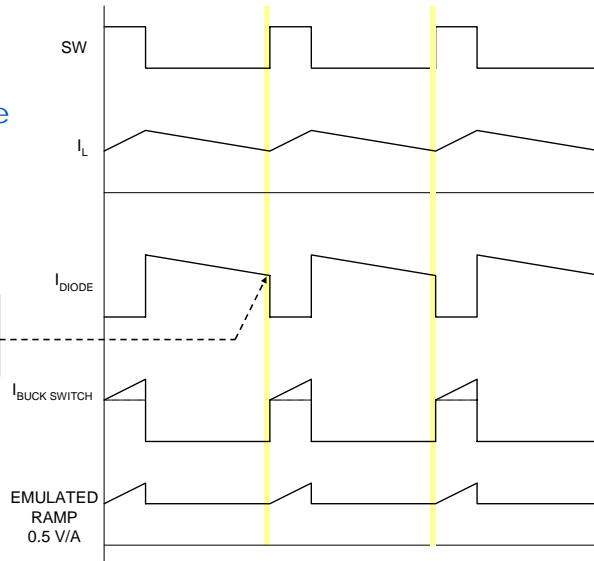


## Emulated Current Mode Waveforms

Emulated  
Current Mode  
Controller  
Timing

Sample and Hold  
of Diode (Inductor)  
Current

 **National  
Semiconductor**  
*The Sight & Sound of Information*



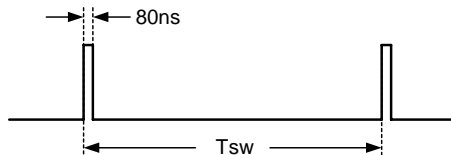
8

Shown on this slide is a timing diagram for the buck regulator power stage. You can see how the inductor current is the sum of the buck switch current and the diode currents. The sample and hold is accomplished at the times indicated by the yellow bars. This sample and hold establishes the pedestal level. Shown on the bottom is the emulated ramp signal scaled to 0.5 V/A.



## Maximum Input Voltage vs Operating Frequency

- With a minimum on-time capability of 80ns, the minimum duty cycle is therefore  $80\text{ns} \times F_{\text{sw}}$ . For low output voltage, high frequency applications the maximum switching frequency may be limited. If  $V_{\text{in}_{\text{MAX}}}$  is exceeded pulses will have to skip.



To calculate the maximum switching frequency use:

$$F_{\text{sw}_{\text{MAX}}} = \frac{V_{\text{out}} + V_{\text{D}}}{V_{\text{in}_{\text{MAX}}} \times 80\text{ns}}$$



Where  $V_{\text{D}}$  is the diode forward drop

9

Applications requiring a high operating frequency along with a large step-down ratio require the controller to have the ability to control the smallest possible minimum on-time. For applications with a large  $V_{\text{in}}$  and a small  $V_{\text{out}}$  the minimum on-time may limit the maximum frequency.

Our new simple switcher regulators can achieve an on-time of 80ns.

The equation for the maximum switching frequency vs  $V_{\text{out}}$ ,  $V_{\text{in}}$  and  $T_{\text{on}}(\text{min})$  is shown.

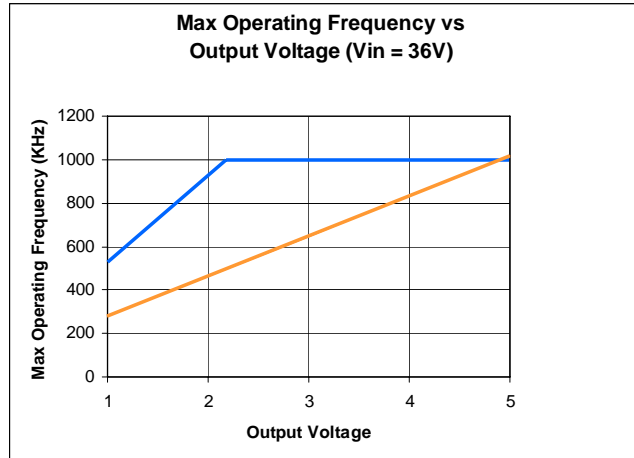


## Maximum Operating Frequency vs Output Voltage

For high input voltage applications the real maximum operating frequency is determined by the minimum on-time ( $T_{ON(MIN)}$ ) of the controller.  
 $F_{SW} = (V_{out} + V_d) / (T_{ON(MIN)} \times V_{in})$

Max operating frequency vs output voltage for the LM2557X family.  
( $T_{ON(MIN)} = 80\text{ns}$ )

Max operating frequency vs output voltage for a "2.8MHz" device.  
( $T_{ON(MIN)} = 150\text{ns}$ )



10

Shown on this graph is a plot of max operating frequency versus output voltage for two different IC regulators with the input voltage set to 36V.

Due to the minimum on-time constraints that we discussed on the previous slide, if the input voltage is set relatively high (in this case 36V) the operating frequency may be limited, depending upon the output voltage.

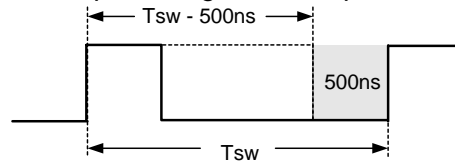
Shown in blue is the maximum operating frequency versus output voltage for the LM2557X family of switching regulators. These devices have a maximum rated operating frequency of 1MHz with a minimum on-time of 80ns.

Shown in orange is a competitor device with a maximum rated operating frequency of 2.8MHz, yet this device has a minimum on-time of 150ns. If the input voltage is set to the maximum of 36V and the output voltage is set to 3.3V this device can only operate to 700KHz, far less than the claim of 2.8MHz.



## Minimum Input Voltage vs Operating Frequency

- A forced off-time of 500ns is implemented each cycle, to allow time for the sample & hold of the diode current. The maximum duty cycle is therefore limited to;  $1 - (500\text{ns} \times F_{\text{sw}})$ . For high frequency applications the minimum input voltage may be limited. If  $V_{\text{in}}$  is less than  $V_{\text{in}_{\text{MIN}}}$  the output voltage will droop.



To calculate the minimum input voltage use:

$$V_{\text{in}_{\text{MIN}}} = \frac{V_{\text{out}} + V_{\text{D}}}{1 - F_{\text{sw}} \times 500\text{ns}}$$

Where  $V_{\text{D}}$  is the diode forward drop

On the past two slides we looked at how the operating frequency may be limited due to minimum duty cycle, caused by the minimum on-time.

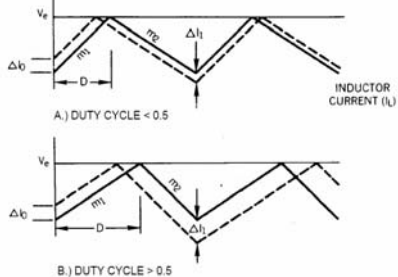
At the other extreme, if the controller's maximum duty cycle is limited to anything less than 100%, then the maximum operating frequency may be limited and the minimum input voltage may be limited.

For the emulated current mode control concept there is a forced off-time each cycle of 500ns. This forced off-time is necessary to allow time for the sample & hold of the diode current. This forced off-time creates a maximum duty cycle limit of  $1 - (500\text{ns} \times F_{\text{sw}})$ . Ideally for a buck regulator the output will remain in regulation even when the input voltage is reduced to almost equal the output voltage. The maximum duty cycle limit requires the input voltage be higher than the output voltage. The minimum input voltage predicted in the equation is lowest input voltage while the output voltage can remain in regulation.

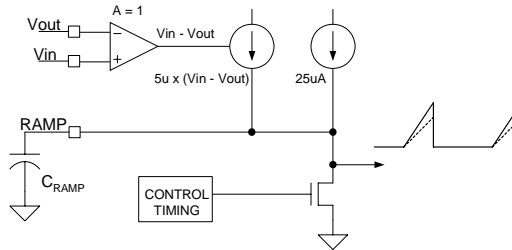


## Slope Compensation

**Background:** Current mode controlled power converters operating at duty cycles  $>50\%$  are prone to sub-harmonic oscillation. Disturbances in peak rising current ( $\Delta I$ ) increase at the end of the cycle.



**Solution:** A  $25\mu\text{A}$  offset in the RAMP current source provides additional slope for the emulation ramp.



Current mode controlled power converters operating at duty cycles  $>50\%$  are prone to sub-harmonic oscillation. Disturbances in peak rising current ( $\Delta I$ ) increase at the end of the cycle causing alternating large and small duty cycles.

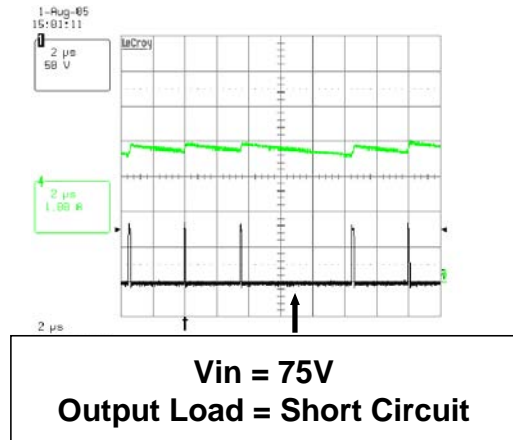
Fortunately, the solution to the sub-harmonic issue is easy to solve. The most common solution is to add additional fixed slope to the current sense ramp. Usually the fixed slope ramp is derived from the oscillator. For the ECM control method a  $25\mu\text{A}$  offset in the RAMP current source provides additional fixed slope for the emulation ramp.



## Robust Over-Current Protection

- An additional benefit of ECM is “look-ahead current limiting” since the inductor current is measured prior to the buck switch on-time.

During high input voltage, extreme short-circuit conditions the buck switch will skip cycles if the inductor current does not decay below the current limit threshold. Skipping cycles prevents the possibility of runaway inductor current.

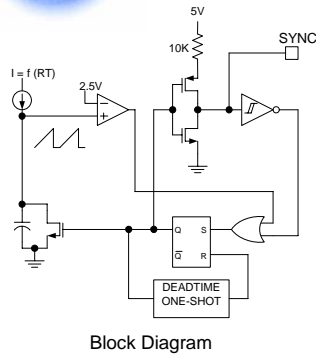


An additional benefit of ECM is “look-ahead current limiting” since the inductor current is measured near the end of the diode conduction time, prior to turning on the buck switch.

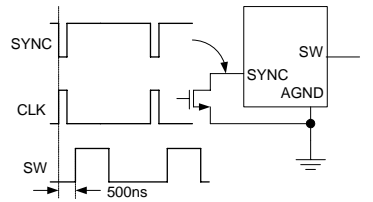
During high input voltage, extreme short-circuit conditions the buck switch will skip cycles if the inductor current does not decay below the current limit threshold. Skipping cycles prevents the possibility of runaway inductor current and provides a very robust over-current protection scheme.



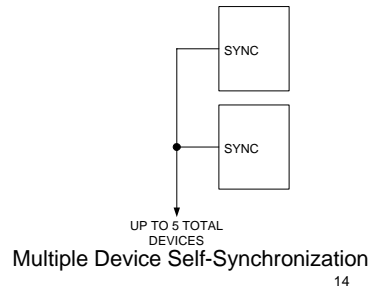
## Oscillator Synchronization



The oscillator can be synchronized to an external clock or multiple devices can be connected together to self-synchronize.



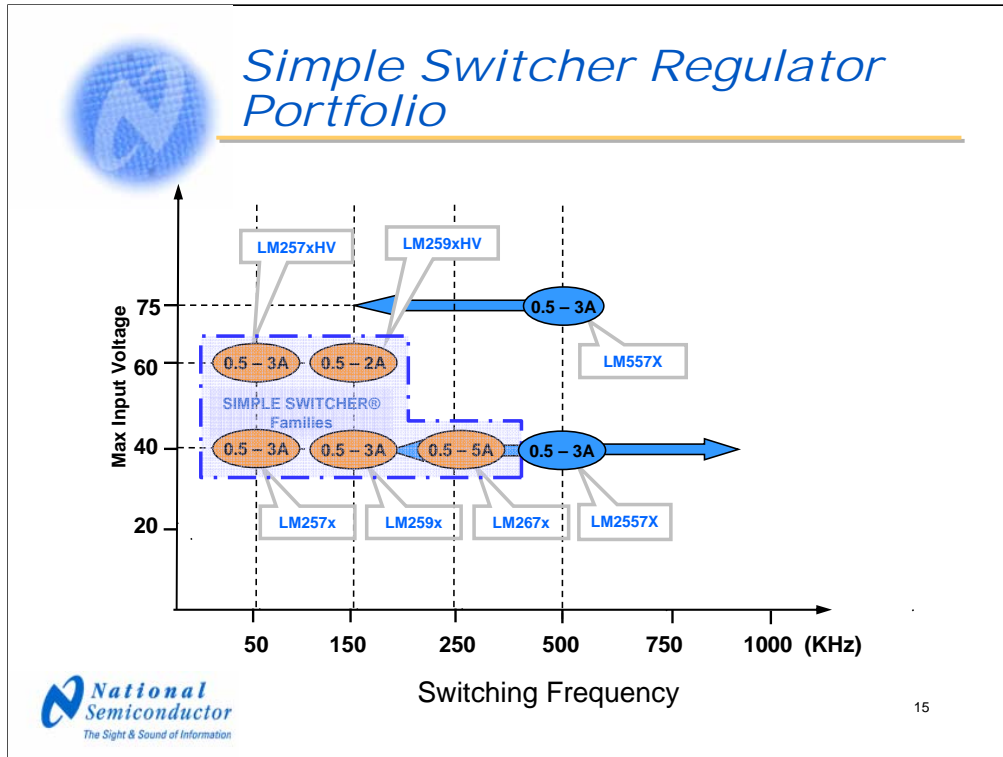
Synchronization to an external clock



Multiple Device Self-Synchronization

14

Each of the newly released regulators has a dedicated oscillator sync pin allowing the regulator to be synchronized to an external clock or like regulators can be connected together to self synchronize. Synchronizing switching regulators reduces system EMI emissions. For the external sync method, an open drain discharge device is necessary as shown. To synchronize like regulators, simply connect the SYNC pins together and the fastest regulator will act as a master while the balance act as slaves.



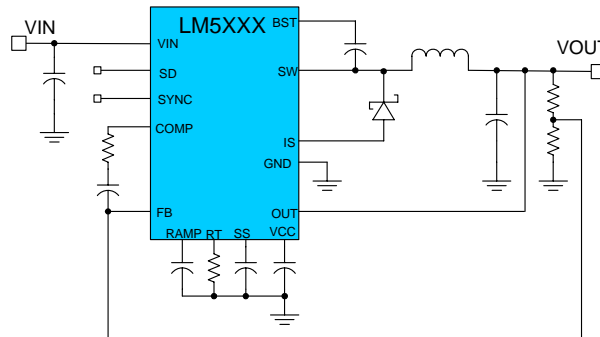
National Semiconductor is a leader in integrated switching buck regulators with a long history. The latest devices utilizing emulated current mode control allow a higher input voltage capability and higher operating frequency than the fixed frequency predecessors. The ability to adjust the operating frequency allows the user to trade-off solution size and efficiency. 500KHz is should a practical maximum for devices rated to 75V while the lower voltage devices can operate from 100KHz to 1MHz.



## Emulated Current Mode Switching Regulators

### Features:

- 75V or 42V Maximum Input Voltage
  - LM(2)5574 - 0.5A
  - LM(2)5575 - 1.5A
  - LM(2)5005 - 2.5A
  - LM(2)5576 - 3A
- 6V Minimum Input Voltage
- Emulated Peak Current Mode Control
- 1.25V  $\pm$  1.5% Voltage Reference
- Adjustable Output from 1.25V
- Single Resistor Frequency Setting
- Oscillator Synchronization Input
- Programmable Soft-start
- Shutdown / Standby Input
- Thermal Shutdown Protection



**Packages:** TSSOP16 (LM5574), TSSOP16-EP (LM5575), TSSOP20-EP (LM5005, LM5576)



16

Shown on this slide is a buck regulator application using one of our new integrated switching regulators. The new family of regulators employs the emulated current mode control technology. There are a total of 8 devices, available with either a 42V or 75V max input voltage and current max current levels of 0.5, 1.5, 2.5 and 3 Amps.

Each device contains a soft start, oscillator sync, remote shutdown capability and thermal shutdown protection. The higher current devices are available in a

TSSOP-EP package with an exposed pad on the underside to aid thermal dissipation.



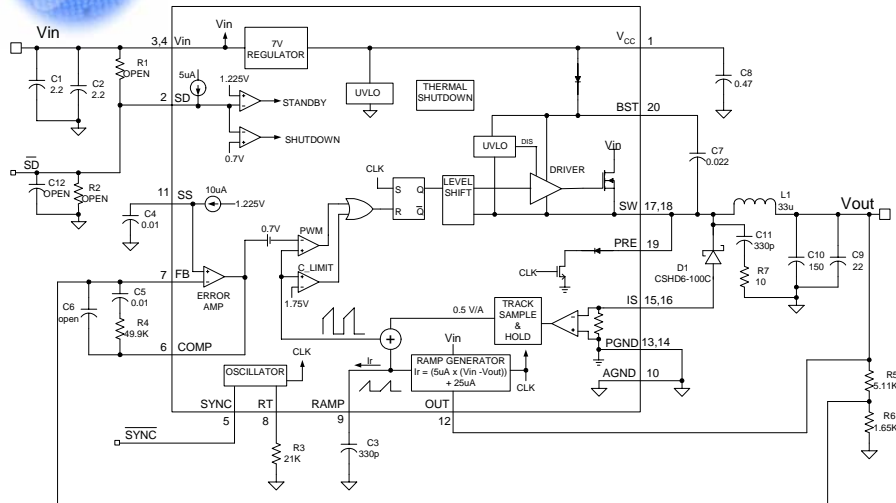
## Simple Switcher ECM Parametric Matrix

NSID	Max Load	Vin Abs Max	Vin Max Op.	Scale Factor (Volts/Amp)	Emulation Current Source	Cramp Equation	I-lim (min)	I-lim (typ)	I-lim (max)	Typ RDSon	Package
LM5574	0.5	76	75	2 V/A	$(10\mu\text{A} \times (\text{Vin} - \text{Vout})) + 50\mu\text{A}$	$\text{Cramp} = L \times 5 \times 10^{-6}$	0.6	0.7	0.85	750m	TSSOP16
LM25574	0.5	45	42	2 V/A	$(10\mu\text{A} \times (\text{Vin} - \text{Vout})) + 50\mu\text{A}$	$\text{Cramp} = L \times 5 \times 10^{-6}$	0.6	0.7	0.85	750m	TSSOP16
LM5575	1.5	76	75	1 V/A	$(10\mu\text{A} \times (\text{Vin} - \text{Vout})) + 50\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	1.8	2.1	2.5	330m	TSSOP16-EP
LM25575	1.5	45	42	1 V/A	$(10\mu\text{A} \times (\text{Vin} - \text{Vout})) + 50\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	1.8	2.1	2.5	330m	TSSOP16-EP
LM5005	2.5	76	75	0.5 V/A	$(5\mu\text{A} \times (\text{Vin} - \text{Vout})) + 25\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	3	3.5	4.25	160m	TSSOP20-EP
LM25005	2.5	45	42	0.5 V/A	$(5\mu\text{A} \times (\text{Vin} - \text{Vout})) + 25\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	3	3.5	4.25	160m	TSSOP20-EP
LM5576	3	76	75	0.5 V/A	$(5\mu\text{A} \times (\text{Vin} - \text{Vout})) + 25\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	3.6	4.2	5.1	170m	TSSOP20-EP
LM25576	3	45	42	0.5 V/A	$(5\mu\text{A} \times (\text{Vin} - \text{Vout})) + 25\mu\text{A}$	$\text{Cramp} = L \times 10^{-5}$	3.6	4.2	5.1	170m	TSSOP20-EP

This matrix is handy guide for selection of the new ECM devices. Shown are the voltage and current ratings as well as scale factors and MOSFET characteristics.



## Block Diagram and Evaluation Board Schematic



Shown on this slide is the detailed block diagram and the evaluation board schematic for a 5 Volt output buck regulator with a 3 Amp current capability. The integrated Buck FET has a 75V rating. The anode of the external diode connects to ground through the regulator's internal current sense resistor. This application operates at a switching frequency of 300KHz.



## Typical Regulator Demo Board

### Performance:

Input Range: 7 to 75V  
Output Voltage: 5V  
Output Current: 0 to 2.5A  
Size: 2.5" x 1" x 0.4"  
Operating Frequency 300KHz  
Oscillator Sync Capability

### Protection:

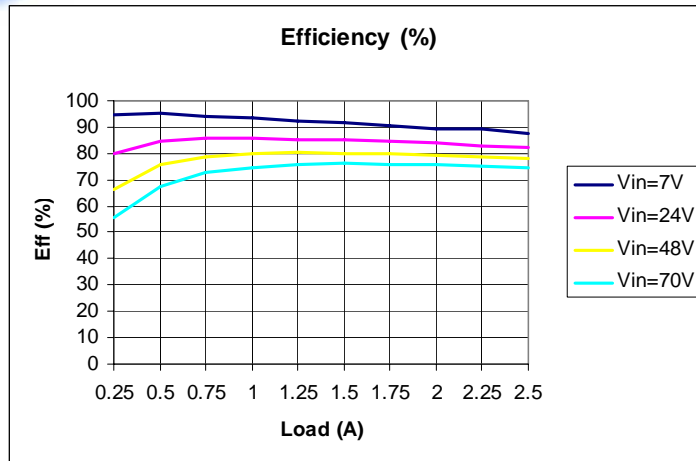
Current Limit Protection  
Thermal Shutdown



Shown on this slide is a picture of one of the available evaluation boards. The schematic for this board was presented on the previous slide.



## Typical Demoboard Efficiency vs. Line and Load

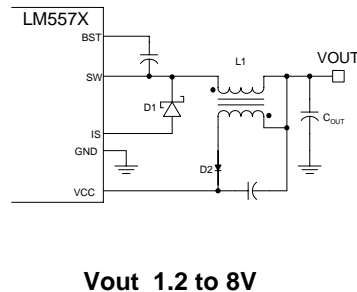
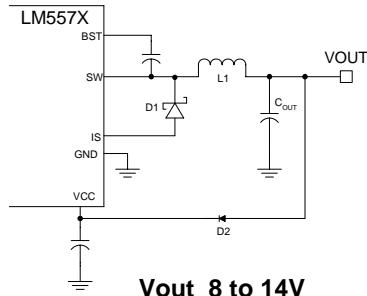


Shown on this slide is an efficiency plot versus line and load for the 2.5A evaluation board. For current levels greater than 1 Amp, the efficiency stays relatively flat while increasing the input voltage has a negative effect upon the efficiency. Increasing the switching frequency would also have a negative effect upon the efficiency. This particular data was taken for a 300KHz design.



## Methods to Provide Bias Power

The LM5576 consumes up to 8mA (300KHz operation) of bias current. At 75V input that's 0.6W dissipated in the controller! Providing bias voltage from the output greatly reduces these losses.

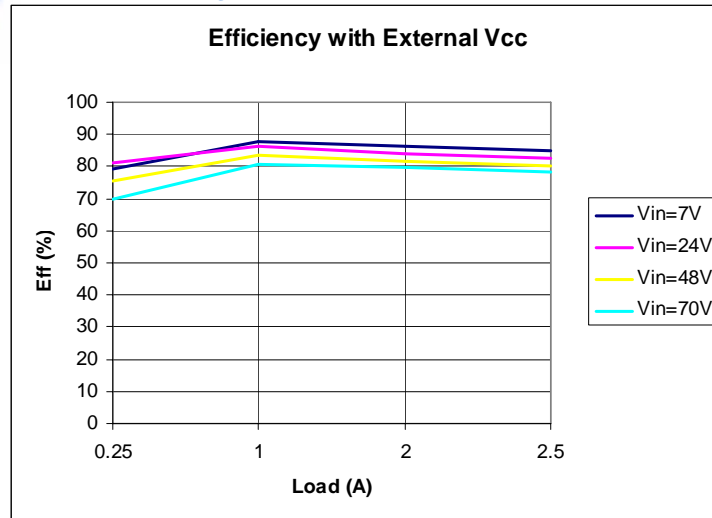


Besides narrow duty cycles, another challenge when designing high input voltage buck regulators is the power lost due to bias power (the power necessary to bias the controller and drive the MOSFET). As an example, the LM5005 consumes up to 8mA (300KHz operation) of bias current. At 75V input that's 0.6W dissipated in the controller! Fortunately there are several ways to reduce this power dissipation. Shown on this slide are two methods of providing bias voltage from the output, greatly reducing the bias power losses.



## Demoboard with External Vcc Efficiency vs. Line and Load

Vcc = 9V



National  
Semiconductor  
The Sight & Sound of Information

Vout = 5V

Fsw = 300KHz

22

Shown on this slide is the same efficiency versus line and load graph that we looked at a few slides back. This graph however was taken with the controller Vcc biased externally. You can see a significant improvement especially at higher input voltages and light loading.



## *Junction-to-Ambient Thermal Resistance*

---

- Junction-to-Ambient thermal resistance,  $\theta_{JA}$  is application dependent. The actual thermal resistance varies with device package type, number and diameter of vias under the exposed pad, area and thickness of the ground plane, quantity of forced air cooling and total PC board power dissipation.
- The units of thermal resistance are  $^{\circ}\text{C} / \text{Watt}$ .
- If you know the power dissipation ( $P_D$ ) of the device then the junction temperature ( $T_J$ ) can be predicted by:  $T_J = T_A + (P_D \times \theta_{JA})$
- In the LM5005 demoboard, there are 5 vias under the regulator IC to connect the underside exposed pad to the ground plane.
- The ground plane has an area of 1.5 in<sup>2</sup> of 2 oz copper.
- Using specialized equipment in a controlled environment, the thermal resistance of the LM5005 demoboard was measured at various air flow rates (Linear Feet per Minute).
  - 0 LFM = 44  $^{\circ}\text{C} / \text{Watt}$
  - 225LFM = 31  $^{\circ}\text{C} / \text{Watt}$
  - 500LFM = 27  $^{\circ}\text{C} / \text{Watt}$
  - 900LFM = 23  $^{\circ}\text{C} / \text{Watt}$

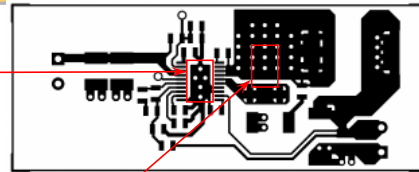
The next few slides will detail several aspects of thermal design.



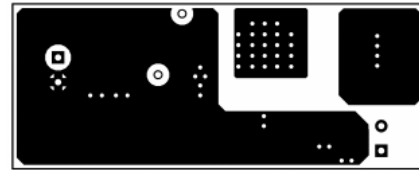
## Typical Demoboard Artwork

Regulator IC

DIODE



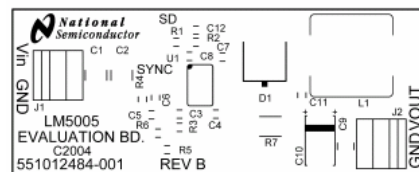
Component Side



Solder Side



**National Semiconductor**  
The Sight & Sound of Information



Shown on this slide is the same 2.5A evaluation board we had looked at earlier. This two layer PC board has several features to aid the thermal design. The two highest dissipating devices are the regulator IC and the diode. Each of these devices have exposed under side pads and the PC board has thermal vias to couple the heat to larger copper areas, aiding power dissipation.



## *Junction-to-Case Thermal Resistance*

---

- Junction-to-Case thermal resistance,  $\theta_{JC}$  has little application dependence.
- The units of thermal resistance are  $^{\circ}\text{C} / \text{Watt}$ .
- If you know the power dissipation ( $P_D$ ) and the case temperature ( $T_C$ ) of the device then the junction temperature ( $T_J$ ) can be predicted by:  
$$T_J = T_C + (P_D \times \theta_{JC})$$
- Junction-to-Case thermal resistance:
  - LM5005, LM5576 6  $^{\circ}\text{C} / \text{Watt}$
  - LM5575 14  $^{\circ}\text{C} / \text{Watt}$
  - LM5574 30  $^{\circ}\text{C} / \text{Watt}$



## Power Losses

---

- The highest power dissipating components are the regulator IC, recirculating diode, inductor and the snubber resistor.
- An approximation for the diode power dissipation is:
  - $I_{OUT} \times V_{FW} \times (1-D)$
- An approximation for the inductor power dissipation is:
  - $I_{OUT}^2 \times R_{ESR} \times 1.3$  (1.3 factor accounts for temperature and ac losses)
- An approximation for the snubber resistor power dissipation is:
  - $V_{IN}^2 \times C_{SNUB} \times F_{SW} \times 0.75$  (0.75 factor accounts for switch losses)
- The IC regulator power dissipation varies with input voltage, output voltage, output current and frequency. The easiest approach is to subtract the output power and other component losses from the input power. More on the next slide. . . .



## *Determining the Regulator Junction Temperature*

---

Objective: Determine the regulator junction temperature.

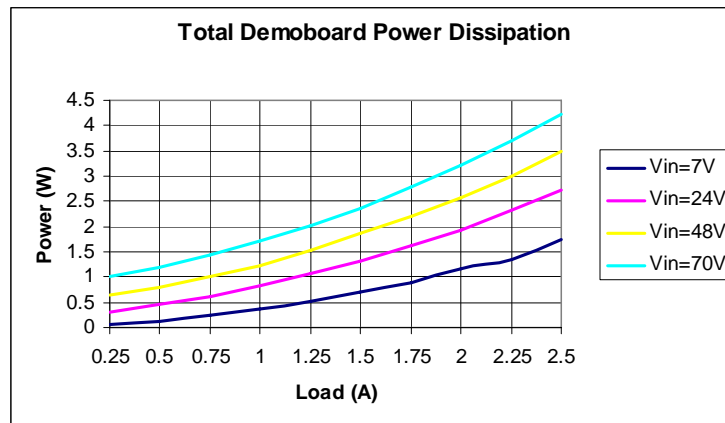
Method:

- Measure the input power ( $P_{IN}$ )
- Measure the output power ( $P_{OUT}$ )
- Calculate the power dissipation of the external components
  - Diode
  - Inductor
  - Snubber
- The IC regulator losses  $P_D$  equal  $P_{IN} - P_{OUT} - P_{DIODE} - P_{IND} - P_{SNUB}$
- Measure the regulator case temperature ( $T_C$ )
- The junction temperature ( $T_J$ ) can be predicted by:  
$$T_J = T_C + (P_D \times \theta_{JC})$$



## Total Power Dissipation vs. Line and Load

$$\text{Total Power Dissipation} = (\text{Vin} \times \text{Iin}) - (\text{Vout} \times \text{Iout})$$

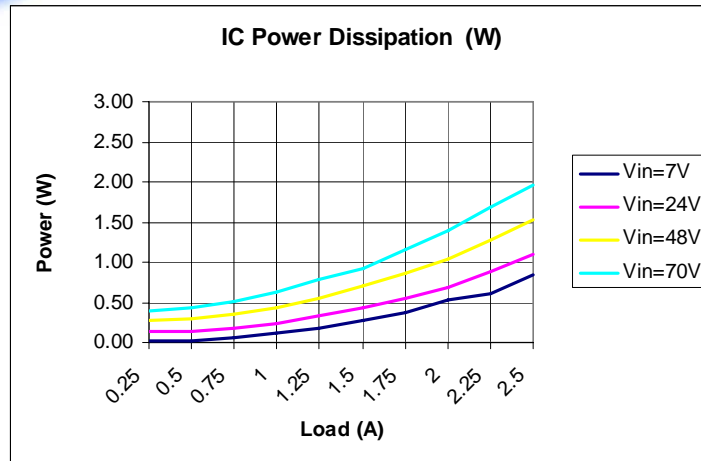


Shown on this slide is first step in determining the regulator junction temperature.

This data is taken from the efficiency graph will looked at earlier. Instead of calculating  $P_{out}$  divided by  $P_{in}$  we are subtraction  $P_{in}$  minus  $P_{out}$ . The difference in power is the total power dissipated in the conversion process.



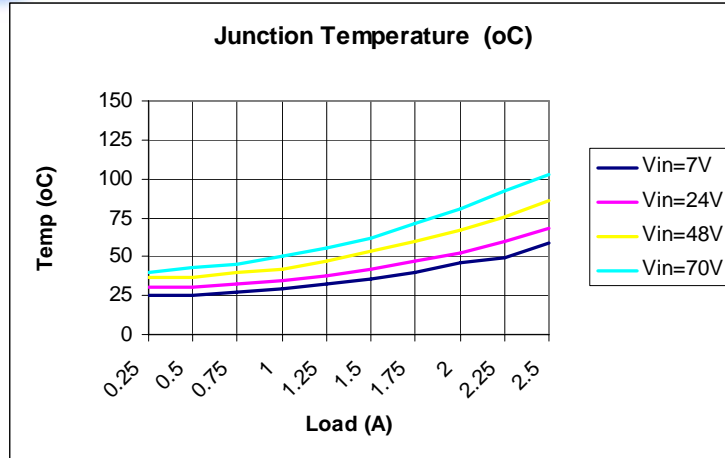
## IC Power Dissipation vs. Line and Load



Taking the previous graph and subtracting the power dissipated in the inductor, diode and snubber leaves the power dissipated in the IC regulator shown on this graph.



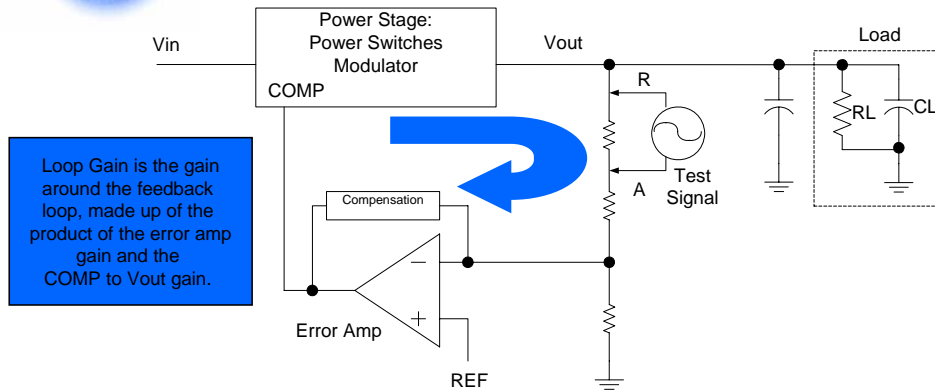
## IC Junction Temperature vs. Line and Load



Finally, if we take the previous graph and multiply by the regulators thermal resistance,  $\theta_{J-C}$ , and adding the measured case temperature leaves us with a graph of junction temperature versus line and load. Generally a typical user need not go through this entire exercise, one or two worst case points will suffice. I did a more rigorous thermal evaluation for illustration.



## Loop Compensation Introduction



Loop Gain is the gain around the feedback loop, made up of the product of the error amp gain and the COMP to Vout gain.

One big advantage of current mode control is the robustness and high performance of the loop dynamics. Current mode control can be modeled as a single pole system. Only the output load resistance and capacitance effect the loop characteristics. The inductor acts as a current source and does not play into the loop dynamics. Another advantage of CM control is that input voltage changes are immediately compensated, referred to as feed-forward.

The first step in understanding loop compensation is to develop an understanding of a good working small-signal model. The term loop gain refers to the gain around the loop shown in blue. This loop can be broken into two parts. First, the power stage is the gain from the COMP input to the output voltage. The DC part of this is simply the load resistance ( $R_L$ ) times the transconductance ( $G_m$ ) of the power stage.

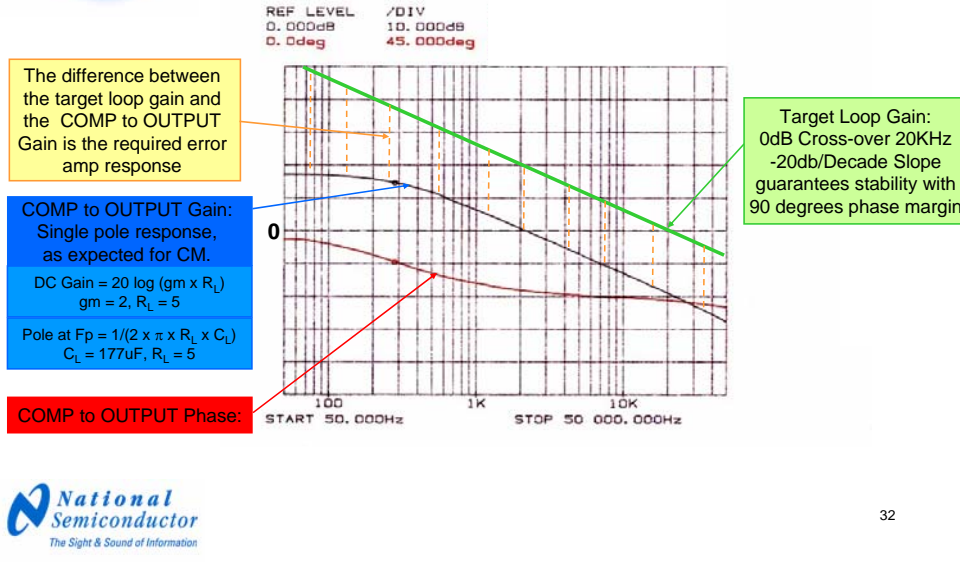
Then there is also a pole at  $1 / 2 \pi R_L C_L$ .

The second part of the loop gain is the error amplifier. The compensation characteristics of the error amplifier have a high DC gain and a zero to compensate the power stage pole.

The next few slides presents a graphical representation of this model.



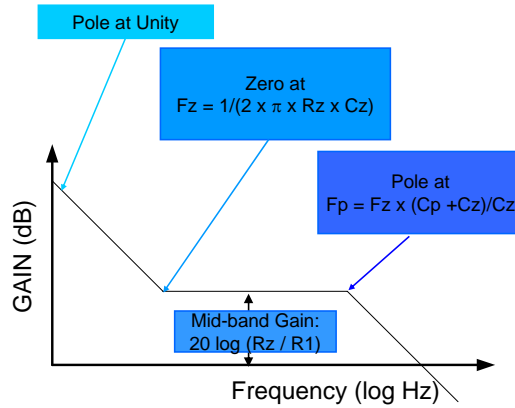
## Loop Compensation



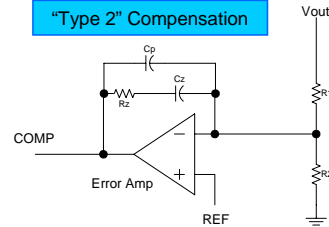
Shown in this slide is a bode plot for a current mode regulator. The units of gain are in dB, remember, addition of terms in dB are the same as multiplication. The loop gain on this plot is the sum of the power stage and the error amplifier gains. If we plot the power stage gain characteristics, shown as COMP to OUTPUT and also draw a target loop gain we can see the desired characteristics of the compensation network as the difference. Selecting an overall loop gain with a slope of -20dB/decade ensures a stable loop with 90 degrees of phase margin.



## Error Amp Design



### "Type 2" Compensation



### Quick Guide:

$$R_z = K \cdot R_{fb1} \cdot C_{out} + \left( \frac{R_{fb1}}{V_{out}} \right)$$

$$K = 2.5 \times 10^5 \text{ (for LM(2)5574)}$$
$$1.2 \times 10^5 \text{ (for LM(2)5575)}$$
$$6 \times 10^4 \text{ (for LM(2)5576)}$$

$$C_z = \frac{1}{8 \cdot 10^3 \cdot R_z}$$

Set  $C_p \leq C_z / 100$  if used

From the previous slide we determined the shape of the error amplifier characteristics. The basic shape requires a high DC gain with a pole at unity and a zero to cancel the power stage pole.

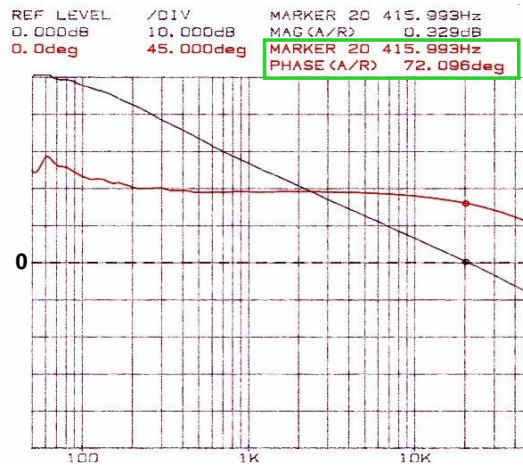
Fortunately, if you did not get all of this I included several quick guide equations on this slide to select compensation components. Also there is an on-line design tool to help select compensation components and view model predictions of the loop. I'll present this tool at the end of the presentation.



## Final Loop Gain Measurements

Gain  
10dB/Div

Phase  
45°/Div



National  
Semiconductor  
*The Sight & Sound of Information*

The final loop gain measurements are shown in this graph. The crossover frequency where the gain equals zero dB is 20KHz and the phase margin at this point is 72 degrees.



## Emulated Current Mode Advantages / Disadvantages

### ADVANTAGES

- Reliably achieves small on-times necessary for large step-down applications.
- All of the intrinsic advantages of current mode control are retained without the noise susceptibility problems often encountered from; diode reverse recovery current, ringing on the switch node and current measurement propagation delays.
- During short circuit overload conditions there is no chance of a current run-away condition since the inductor current is sampled BEFORE the buck switch is turned on. If the inductor current is excessive, cycles will be skipped until the current decays below the over-current threshold.

### DISADVANTAGES

- The maximum duty cycle is limited to less than 100% since off-time is required for the sample and hold measurement of the diode current. There is 500ns of forced off-time each cycle.

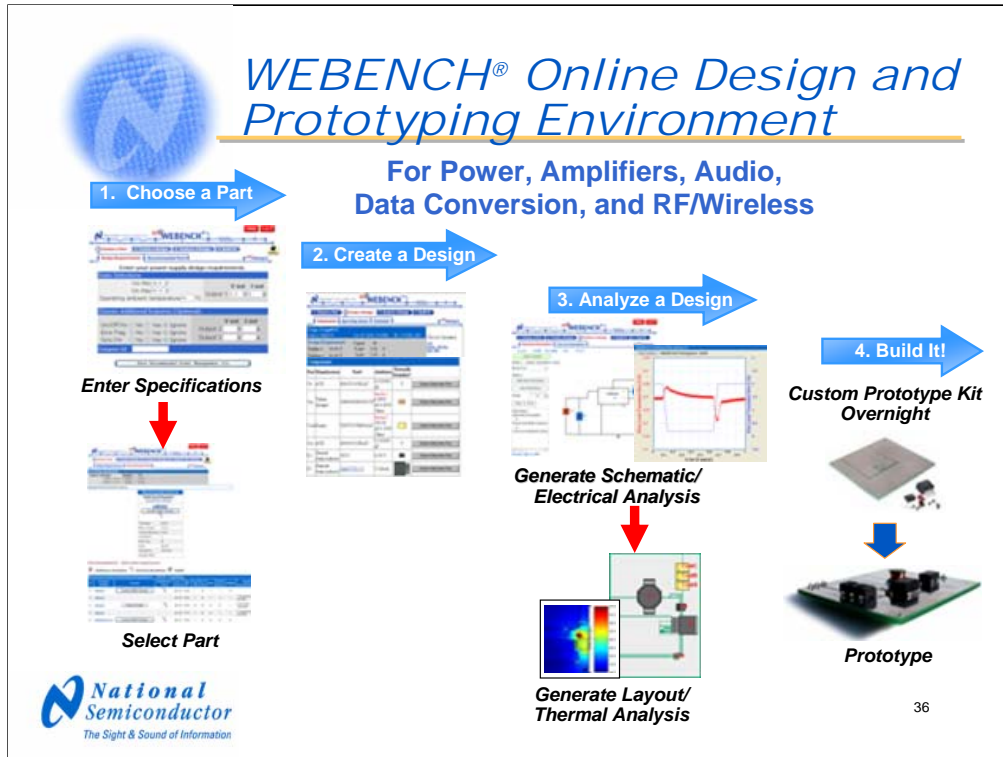
In summary the emulated current mode offers all of the advantages of conventional current mode with the following advantages and disadvantages:

#### ADVANTAGES:

- Reliably achieves small on-times necessary for large step-down applications.
- All of the intrinsic advantages of current mode control are retained without the noise susceptibility problems often encountered from; diode reverse recovery current, ringing on the switch node and current measurement propagation delays.
- During short circuit overload conditions there is no chance of a current run-away condition since the inductor current is sampled BEFORE the buck switch is turned on. If the inductor current is excessive, cycles will be skipped until the current decays below the over-current threshold.

#### DISADVANTAGES:

- The maximum duty cycle is limited to less than 100% since off-time is required for the sample and hold measurement of the diode current. There is 500ns of forced off-time each cycle.

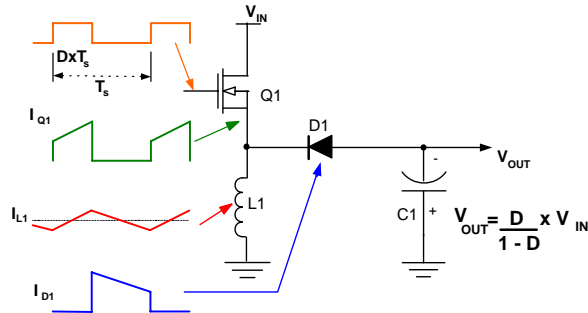


An extensive suite of on-line tools are available on the National Semiconductor website to aid the designer when using the new family of Emulated Current Mode Simple Switchers.

Simply input your design parameters such as input voltage range and output voltage and current. A semi-custom design will be created for you. You can then simulate your design both electrically and thermally. Finally if you wish, a custom prototype kit can be rushed to you overnight.



## Positive Input, Minus Output Buck-Boost Application

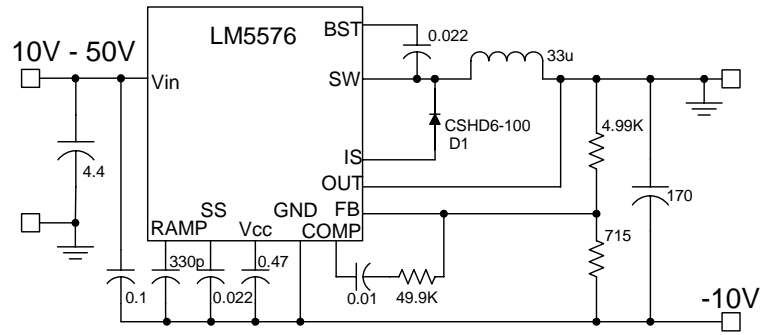


A Buck regulator can be reconfigured into a Buck-Boost regulator to convert a positive input voltage to a negative output voltage. The basic component configuration of a Buck regulator and a Buck-Boost regulator are very similar, with the inductor and the rectifier diode transposed. Since the main switch ( $Q1$ ) is in the same location for each configuration, a Buck regulator IC can be used for either topology. When  $Q1$  is turned on, the input voltage ( $V_{in}$ ) is applied across the power inductor ( $L1$ ). Current in the inductor ramps up during the on-time. When  $Q1$  is turned off the inductor current continues to flow through  $C1$ , the load resistance and  $D1$ , establishing a negative output voltage. During the next  $Q1$  on-time the load is supported by the output capacitor.

Before closing I would like to present a circuit that can be used to create a minus output from a positive input. If you look at this circuit it is similar to the buck regulator except the inductor and diode are swapped. Since the main switch ( $Q1$ ) is in the same location for each configuration, a Buck regulator IC can be used for either topology. When  $Q1$  is turned on, the input voltage ( $V_{in}$ ) is applied across the power inductor ( $L1$ ). Current in the inductor ramps up during the on-time. When  $Q1$  is turned off the inductor current continues to flow through  $C1$ , the load resistance and  $D1$ , establishing a negative output voltage. During the next  $Q1$  on-time the load is supported by the output capacitor.



## Positive Input, -10V Output Buck-Boost Application



- An Emulated Current Mode controlled Buck regulator IC can be reconfigured to the inverting Buck-Boost topology.
- Load current = average inductor current x off-time duty cycle. Therefore the inductor current is higher than the load current.
- Max. input voltage =  $75V - |V_{out}|$

Shown on this slide is a complete schematic for a minus 10V Buck-Boost regulator. The 75V capability of the LM5576 is necessary since the IC “sees” the absolute difference between the input and output voltages for this application.



## Conclusion

---

- Emulated current mode control retains all of the intrinsic performance and ease-of-use benefits found in conventional current mode control, with reduced noise susceptibility and high operating frequency.
- The next generation of Simple Switcher buck regulators utilize emulated current mode control, allowing the user the ability to optimize the solution size and performance.
- These new Simple Switchers are available with output current capabilities of 0.5A, 1.5A, 2.5A and 3A. The maximum input voltage capability is offered as either 42V and 75V.
- An on-line design and simulation tool, Webench, is available for each device.

This concludes my presentation.

Emulated current mode control retains all of the intrinsic performance and ease-of-use benefits found in conventional current mode control, with reduced noise susceptibility and high operating frequency.

The next generation of Simple Switcher buck regulators utilize emulated current mode control, allowing the user the ability to optimize the solution size and performance.

These new Simple Switchers are available with output current capabilities of 0.5A, 1.5A, 2.5A and 3A. The maximum input voltage capability is offered as either 42V and 75V.

An on-line design and simulation tool, Webench, is available for each device.



## ***More information***

Power Management Products

<http://power.national.com>

High-Voltage Switching Regulator Products

<http://www.national.com/appinfo/power/hv.html>

40

More information, such as design tools, application notes, datasheets, evaluation boards and samples can be found on the National website.



---

 ***National  
Semiconductor***  
*The Sight & Sound of Information*