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Hot Swap with Confidence

LM5069 Positive Hot Swap Controller

1

Hello, my name is Neil Gutierrez and I'm here today to talk to you about the LM5069 Positive Hot Swap Controller, Hot Swap with Confidence. The goal of the presentation is to show how a user can use the LM5069 controller to confidently hot swap the application without any fear of damage to the boards or external components.

Webcast Outline

- Hot Swap
- Hot Swap Controller
- Hot Swap Application using external MOSFET
- Safe Operating Area (SOA) and Current/Power Limiting
- LM5069 Features
- Application Plots
- Inductive spike issue

2

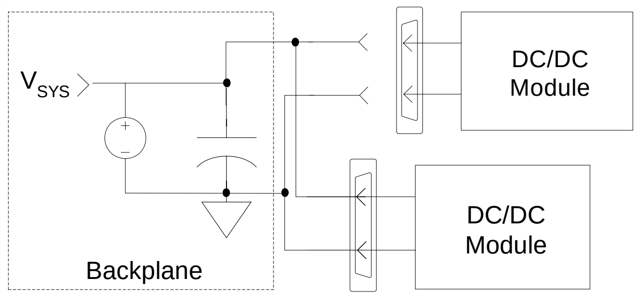
Before I go into the Webcast I would like to go over a brief outline. First, we will define what a hot swap is and what it is used for, what are the benefits of hot swapping and what issues arise from hot swapping. We will then go over the characteristics of a hot swap controller and how it is used in a hot swap application, plus other uses of the controller, other than the hot swap application. We will then go through a specific hot swap application using an external MOSFET as an active switch to isolate the backplane from the secondary modules.

Now, when using an external MOSFET in a hot swap one needs to understand the importance of the safe operating area of the FET, how current and power limiting interact with the SOA curve and what problems can occur. We will then discuss the features of the LM5069 and how it meets the criteria of a hot swap controller as well as keeping the external FET within the SOA.

We will then go through real world data of various scope plots highlighting the features of the LM5069 positive hot swap controller and we'll conclude with the inductive spike issue on the input line and how to suppress them.

So, what is hot swapping?

Why use a Hot Swap?



- **Hot swapping helps reduce system down time when removing and inserting boards into a backplane since shutting down the backplane power is not necessary.**
- **This in turn keeps the backplane power available to other modules when removing faulty boards from the system.**

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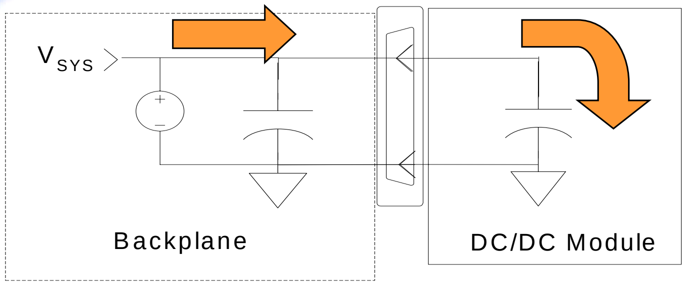
4

What is shown here is a block diagram showing a system backplane voltage and DC modules connected to it. Now, the definition of hot swapping is to physically insert and remove other DC to DC modules into a live backplane. Why would one do this? Well, hot swapping helps reduce system downtime when removing and inserting boards into a backplane, since shutting down the backplane power is not necessary. This in turn will keep the backplane power available to other modules when removing faulty boards from the system.

Issues of Hot Swap



- **Large capacitors on the DC/DC module provide an initial low impedance path when plugged into the backplane.**
- **Simply inserting the secondary boards into the backplane causes large in-rush current**

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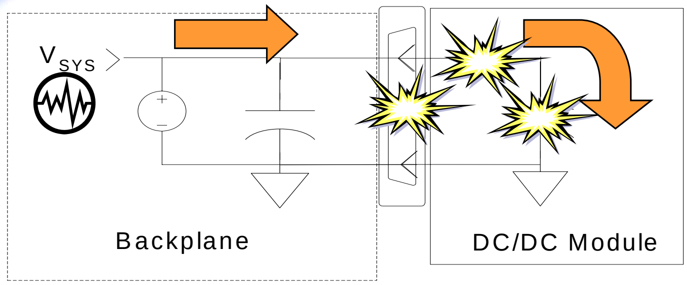
5

Now, what issues arise from hot swapping? When you first insert a module into a backplane, large capacitors on the DC to DC module will provide an initial low impedance path when plugged into the backplane. This causes large inrush currents to go from the system backplane voltage to your DC to DC modules.

Issues of Hot Swap



- **The large in-rush currents can damage connectors, trace lines and capacitors**
- **With the large current surge, system voltages may momentarily fall, resetting other boards.**

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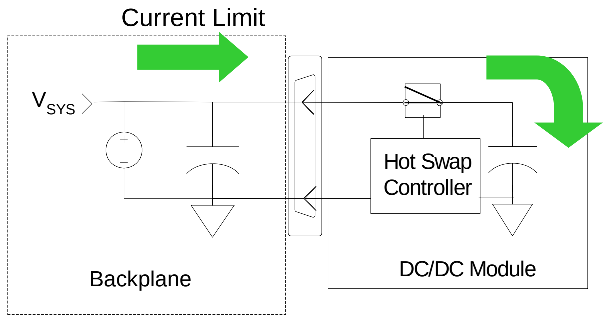
6

Now, what happens is that these large inrush currents can damage connectors, trace lines and capacitors. Another issue is that the large current may cause the system voltage to fall and reset other boards, which is unwanted.

Now, with the issues of hot swapping some sort of hot swap controller is needed.

Hot swap controllers



- Hot Swap controllers are used to control inrush current
- Controlling the inrush current avoids collapsing the backplane and resetting other secondary boards

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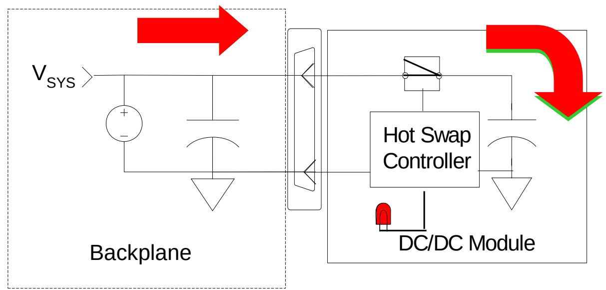
8

So, what you see here is the same diagram as shown before, but instead we've added a hot swap controller along with a switch. So, the hot swap controller would be used to control this inrush current to a current limit and controlling this inrush current will avoid collapsing the backplane and resetting other secondary boards.

Hot swap controllers

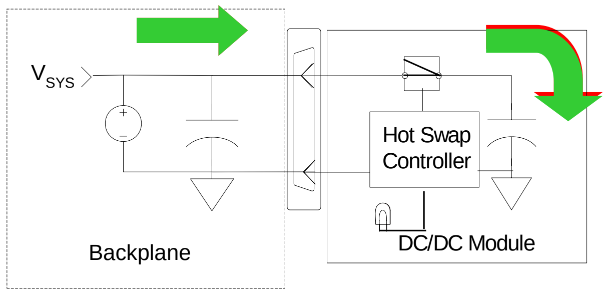


- **Hot Swap Controllers can isolate faulty boards from the backplane and flag them for repair**

9

Now, another feature of the hot swap controller is that if during normal operation the current were to increase beyond the current limit, the hot swap controller can isolate this faulty board and flag them for repair.

Hot swap controllers

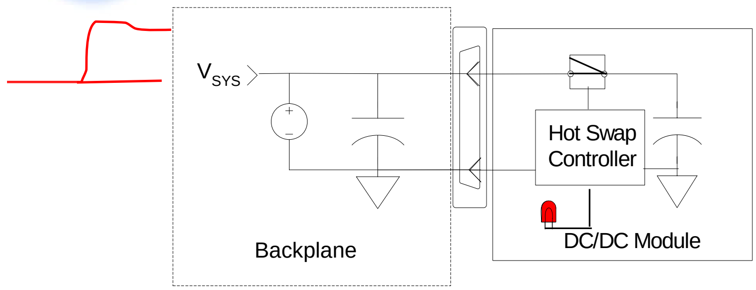


- Controllers can disable a board due to an intermittent short
- Then re-enable the board when the short is removed

10

Another feature of the hot swap controller is that, again, during normal operation if the current were to increase because of an intermittent short, it would flag it for repair and open it up. However, if the short went away the part will re-enable the board when the short is removed.

Hot swap controllers



- **Hot Swap controllers monitor backplane voltage and isolate modules when backplane voltage is out of specification**

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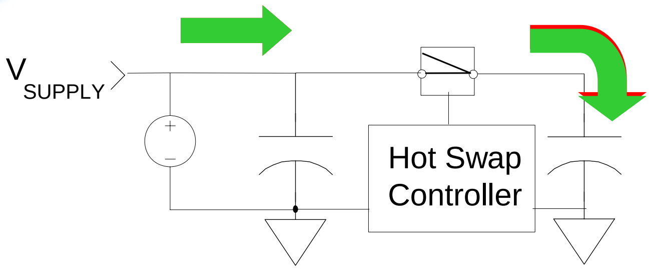
11

Another feature of the hot swap controller is that it monitors the system voltage. If at any time the system voltage were to increase or decrease beyond a certain range, the hot swap controller can isolate the DC to DC module away from this backplane voltage.

Hot swap controller in other applications

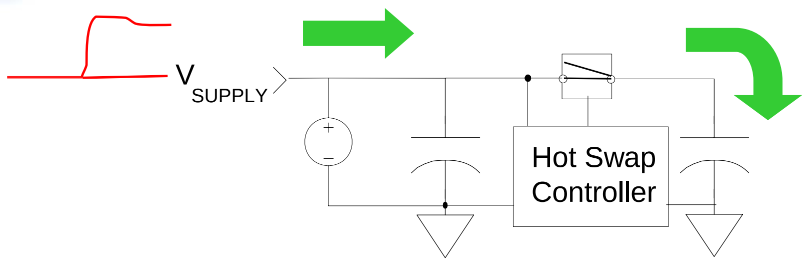


- **In general, the controller can be used in any application where there is a need for a current limit**

12

Now, we’ve shown that the hot swap controller is used in a hot swap application, but any application where there is a need for a current limit, the controller can be used.

Hot swap controller in other application



- **The controller can also be used in any application with a need for over-voltage sensing**

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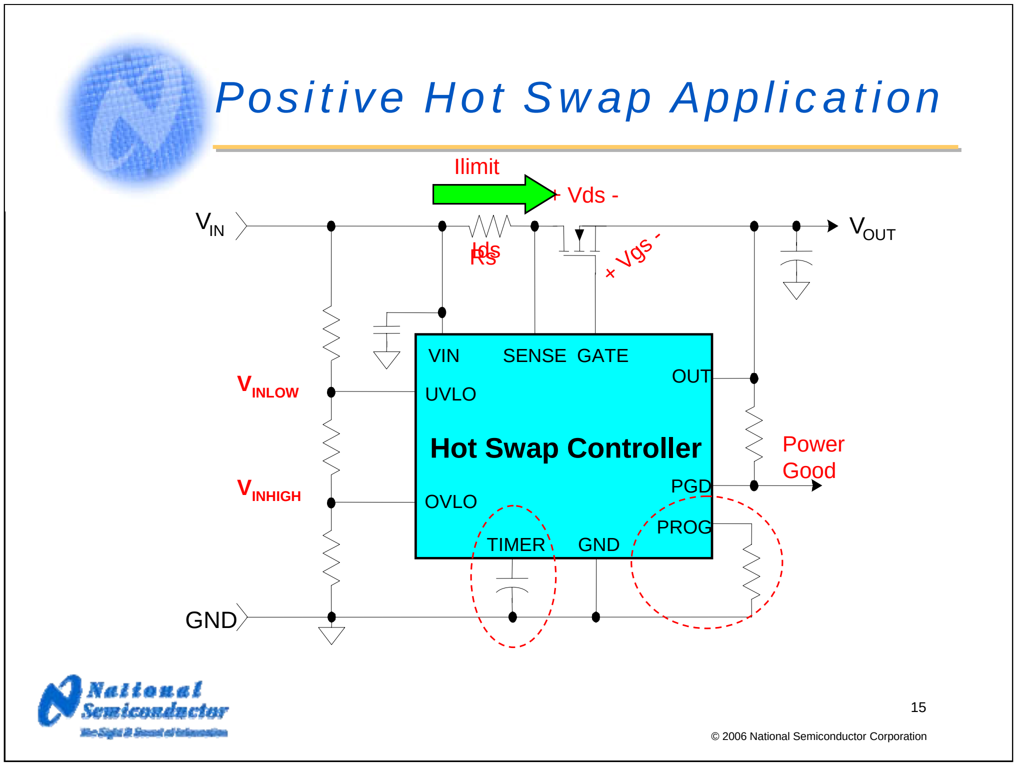
13

This in turn goes as well for any application where there is a need for an over-voltage type monitoring. It can then isolate that system voltage away from your output.

Let’s go over a specific hot swap application using a controller and an external FET. The external FET replaces the switch that was shown earlier.



So, what is shown here is that application. We have a controller with an external FET with a sense resistor and some other sensing resistors. Now, the inrush current is controlled by modulating your gate voltage and keeping it in a current limit. Now, you can see that the input is trying to get to the output, but in order to enhance the FET, the gate voltage has to increase above the input voltage so the controller will have some sort of internal charge pump to pump up this voltage.

Now, current limiting is sensed through the sense resistor and will produce a maximum voltage across the sense resistor. Once that is detected the gate will stay at that point to keep the current at the current limit. Under voltage and over voltage of the input voltage is sensed through a resistor divider to the UVLO and OVLO pins respectively. It checks to make sure that your input voltage is within a specific range, that it is above the under-voltage threshold and below the over-voltage threshold. If any of those cases are violated the gate will shut off.

The timer pin has two functions. One is for initial insertion, which is when you first insert the module, there is a lot of ringing and transients on your input voltage to the part. So, we want that amount of time to have it settle down. So, the insertion time, nothing will happen on the gate, it will be off during this time so that input voltage can settle. The other function of the timer is that of a fault time out. So, during a current limit or power limit there is a set amount of time set by this timer capacitor, which is allowed. After that time the gate will shut off.

The program pin is used to program your power, more on that will be said on the LM5069.

The PGD pin is your power good pin. This is your indicator to show that your power is good, meaning that your output has reached its input voltage to a specified range. It can then be used to flag downstream DC to DC converters and start bucking.

Hot Swap Application

- Controls the inrush current by modulating the Gate voltage
- Charge pump on the Gate is necessary for enhancing the external FET
- Current limit is programmed via the sense resistor (Rs)
- Input undervoltage and overvoltage are sensed at the UVLO and OVLO pins, respectively
- Allowed fault time is programmed through the TIMER circuit via a charge current and capacitor
- Allowed power limit is programmed by the PROG resistor
- Output voltage is “good” indicated by Power Good signal

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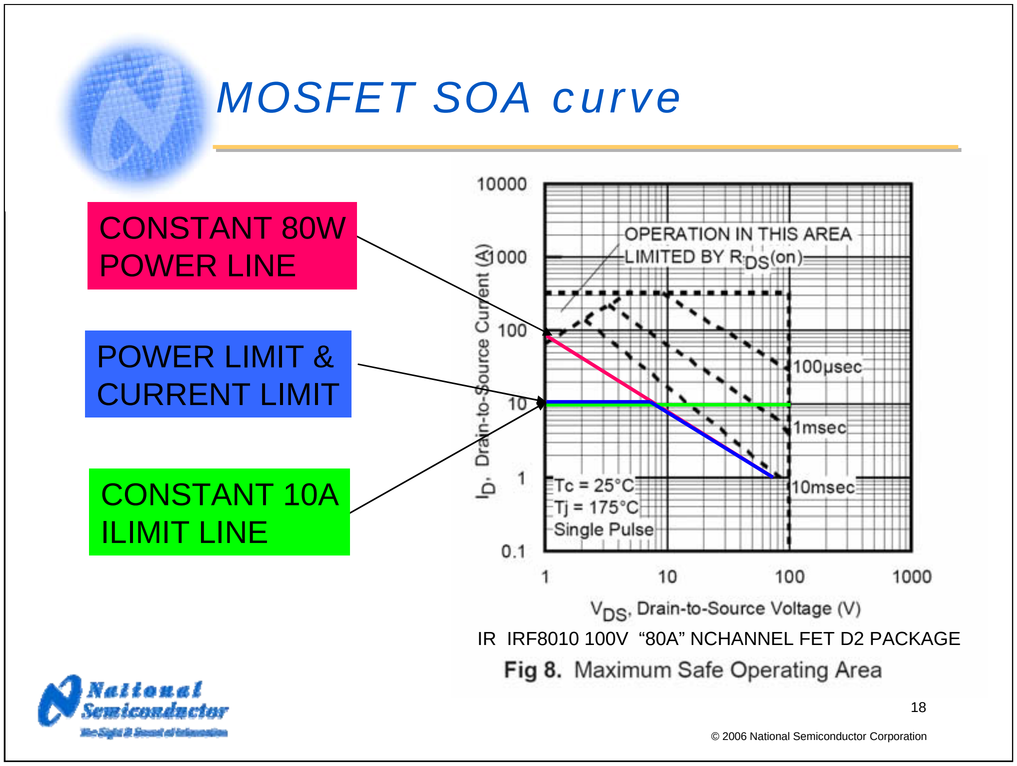
16

All the things that I’ve stated are summarized in this slide, which can be used by the user at a later time.

Now, using the hot swap controller with an external MOSFET can limit the inrush current and protect the DC to DC module. However, the external MOSFET itself needs to be protected as well. Looking at the MOSFET's safe operating curve will give us some insight in how to protect the external FET.



So, what is shown here is your typical SOA curve. It has a max breakdown of 100 volts Vds and at low Vds the current is limited due to the RDSON of the FET. Your max current is limited due to just package thermal limits. Now, curves shown with time show the energy limitations of the FET. For example, when Vds is less than 12 volts a current pulse lasting 10 milliseconds is limited to 10 amps. Currents larger than 10 amps may damage the FET because you are outside the safe operating area. Typically, the hot swap controller can control current, power or a combination of both. But as you can see, there are problems associated with just limiting current or power.

Hot Swap with Current Limit only

- 10A Current limit into 1000uF
  - IDS = C * dV/dt →
    10A = 1000uF * 80V / dt →
    dt = 8ms
  - Current pulse will last 8ms
  - Initially at 80V VDS and 10A IDS the MOSFET is <u>outside the safe operating area (SOA)</u>
  - Until the VDS < 15V, the MOSFET will be outside of the SOA.

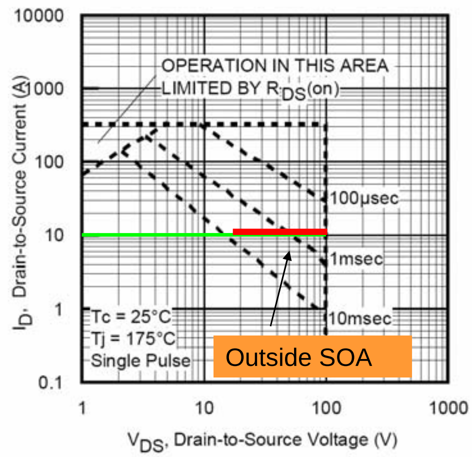


Fig 8. Maximum Safe Operating Area

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19

So, let's take an example. Here we have an example of a current limit. We are going to limit to 10 amps, our output capacitor is at 1,000uF. Now, simply using I=C * dV/dt, we can see that the current pulse will last eight milliseconds. The problem is, initially at 80 volts Vds, let's say your input voltage is 80 volts, you are going to limit to 10 amps, but the MOSFET is outside the safe operating area. Until the Vds decreases to less than 15 volts, the MOSFET will be outside of the SOA.

Hot Swap with Power limit only

- Power limit into 1000uF
  - IDS * VDS = 80W
  - Current will start from 1A IDS at 80V VDS and has a 80A IDS at 1V VDS
  - MOSFET stays inside of the SOA.
  - <u>Peak currents get large at small VDS</u>

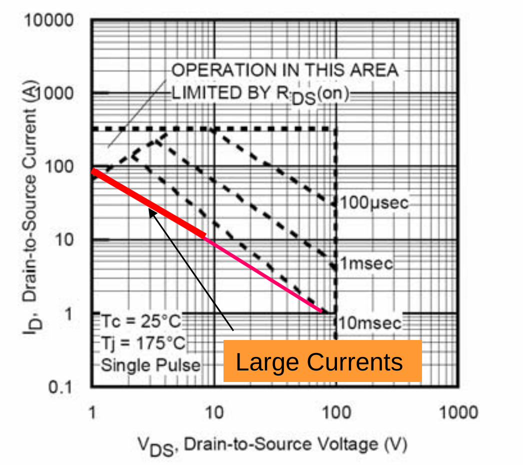


Fig 8. Maximum Safe Operating Area

20

Now, if you are power limiting into this same 1,000uF cap we will set it to 80 watts. This time the current will start from 1 amp at 80 volts Vds, but increase up to 80 amps at one volt Vds. The MOSFET stays inside of the SOA, but your peak currents get large at small Vds.

Hot Swap with Power limit and Current limit

- Power limit and current limit into 1000uF
  - Ids * Vds = 80W and Ids max = 10A
  - Current will start from 1A Ids at 80V Vds and limit to 10A Ids at 8V Vds
  - At Vds < 8V, Ids limited to 10A
  - <u>MOSFET stays inside of the SOA and peak current stays low</u>

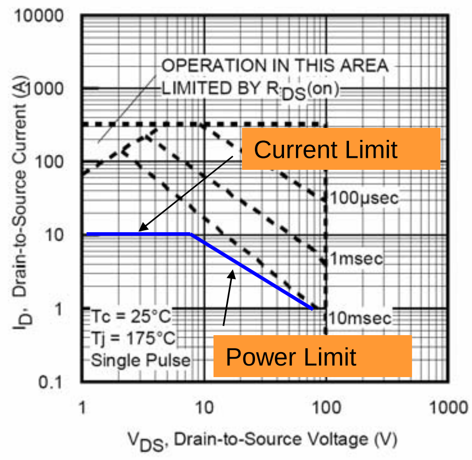


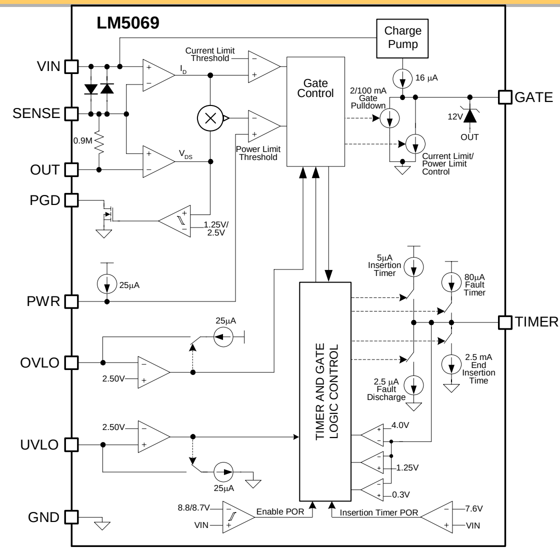
Fig 8. Maximum Safe Operating Area

21

So, with a combination of both into the same application of 80 watts power and 10 amps max, we'll first start out, like before, one amp at 80 volts Vds and limit to 10 amps at eight volts Vds. Anything less than eight volts the current will be limited to 10 amps. So, you can see that we get the best of both worlds. The MOSFET stays inside the SOA and the peak current stays low.

We will now go over the features of the LM5069 and how it implements the prior characteristics of the controller to confidently hot swap.

LM5069 Positive Hot Swap Controller with Power Limiting

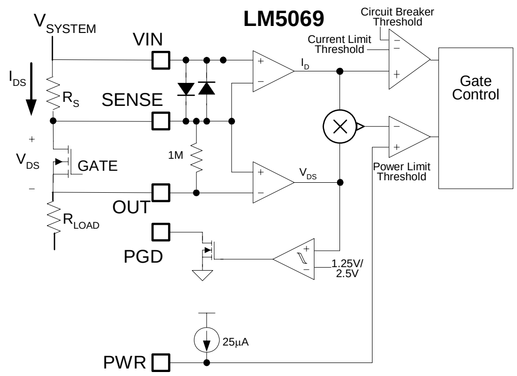


23

What is shown here is the block diagram of LM5069. This is taken from the datasheet. We will highlight the current and power limiting area, the power good circuitry, the gate drive, UVLO and OVLO, under-voltage and over-voltage lockout, and the timer circuitry.

LM5069 Positive Hot Swap Controller with Power Limiting

- In-rush current is limited for safe board insertion into live backplanes
- Current is limited either by the adjustable power limit through PWR or by the maximum current limit sensed by Rs
- Includes an active high open drain PGD (Power Good) output
- Includes a circuit breaker function to prevent over current conditions

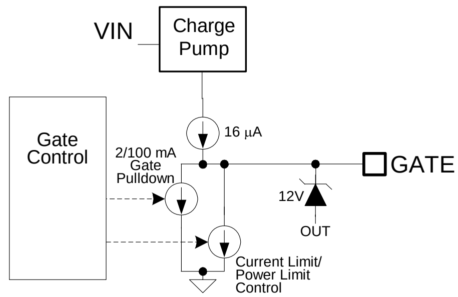


24

So, let's first go over the power limiting and current limiting. So, the inrush current is limited by the controller so that you can safely insert the board into the live backplane. Now, the current is either limited by the power limit or through the maximum current limit sensed by Rs. We also included the PGD pin, now remember this is the PGD pin that is used to indicate that the output is ready to be used by the downstream DC to DC converters. And in this case when the output voltage is within 1.25 volts of the input voltage, the PGD pin is – or the open drain is de-asserted and any pull up on it will get asserted and show that it is ready to be used. Now also included is the circuit breaker function and this is to prevent over current conditions. So, what happens is, if there is a large inrush current such that it doesn't get limited by the current limit or power limit because of bandwidth issues, it will go to the circuit breaker threshold and that will immediately shut off the gate to limit the current.

LM5069 Positive Hot Swap Controller with Power Limiting

- Internal high side charge pump and driver for external N-channel MOSFET
- 100mA pull-down on GATE at initial insertion to prevent turn on of external N-channel MOSFETdue to gate to drain capacitance



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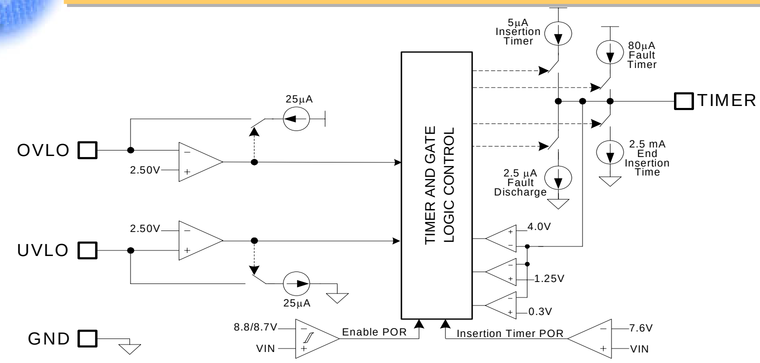
25

Now, I stated before that in order to enhance the external N-channel FET there is a need for a charge pump and that is what is shown here with a 16 microamp pull up. The gate is limited to be 12 volts above the input voltage due to the zener clamp from gate to out. Also included is the 100 milliamp pull down on the gate and that is used for initial insertion to keep the N-channel MOSFET off and that is due to the gate to drain capacitance, the miller capacitance. Remember, when you first insert the board there is large Dv/Dt's that can occur on the input and enhance the FET. So it is imperative to keep that gate low and that is what the 100 milliamp pull down is for.

LM5069 Positive Hot Swap Controller with Power Limiting



- **Adjustable under-voltage lockout (UVLO) and hysteresis**
- **Adjustable over-voltage lockout (OVLO) and hysteresis**
- **Initial insertion timer allows ringing and transients to subside**
- **Programmable fault timer avoids nuisance trips**

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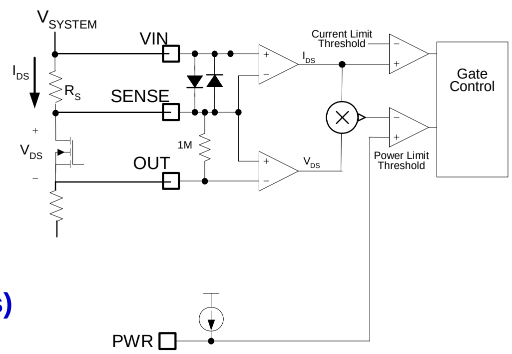
26

This next slide is showing the under voltage and over voltage circuitry. Remember that a resistor divider is monitoring the input voltage and are sent to the OVLO and UVLO pin to make sure that they are within range. If they are within range the gate is allowed to enhance.

The timer part of this circuitry is, again, the initial insertion time, which is allowing for ringing and transients to subside and that is with a five microamp insertion current. The fault timer is also programmed through this timer pin and can avoid those nuisance trips, but remember that fault time is programmed to show how long a user will tolerate a fault, either a current limit or a power limit.

Who limits the current?

- **Ids is limited by Ilimit:**
  Ilimit = 50mV / Rs
- **Ids is limited by Plimit:**
  Plimit = 8.2uW * Rpwr / Rs
  Since Plimit = Ids*Vds
  Ids * Vds = 8.2uW * Rpwr / Rs
  Ids = 8.2uW * Rpwr / (Rs * Vds)
- **With varying Vds, the FET current is limited to Ids or Ilimit, whichever is smaller**



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27

So, who limits the current? Well, the current is limited either by current limit, which is a maximum of 50 millivolts that is sensed through the sense resistor or it's programmed by a ratio of the power resistor to the sense resistor and will limit the Ids that way. Now, with varying Vds the FET current is limited to either the Ids due to power or Ilimit whoever is smaller.

Who limits the current?

- **Example**
  - **Ilimit = 10A → Rs = 50mV / 10A = 5mΩ**
  - **Plimit = 80W → Rpwr = Plimit * Rs / 8.2uW**

    = 80W * 5mΩ / 8.2uW

    = 48.8kΩ

Current limit set to 10A with Rs = 5mΩ
Power limit set to 80W with Rpwr = 48.8kΩ

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28

So, let's look at an example. So, I want to current limit to 10 amps, so that tells me that I need to choose a sense resistor that is five milliohms. Since the sense resistance is five milliohms, I can now program my power pin to be 48.8k for an 80 watt power limit. So, we have a current limit that is set to 10 amps with a sense resistor of five milliohms, a power limit that is set to 80 watts, with a power resistor of 48.8k.

Power limit and Current limit Operation

- Power limit and current limit into 1000uF
  - Ids * Vds = 80W and Ids max = 10A
  - Current will start from 1A Ids at 80V Vds and limit to 10A Ids at 8V Vds
  - At Vds < 8V, Ids limited to 10A
  - <u>MOSFET stays inside of the SOA and peak current stays low</u>

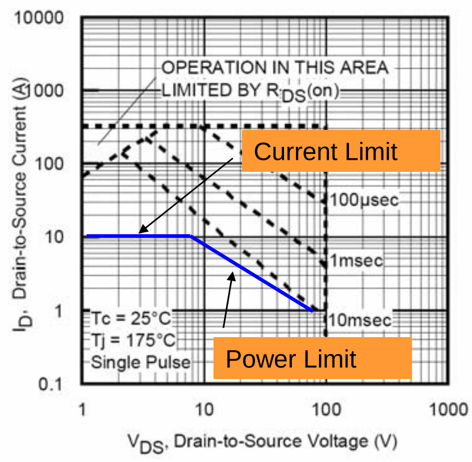

Fig 8. Maximum Safe Operating Area

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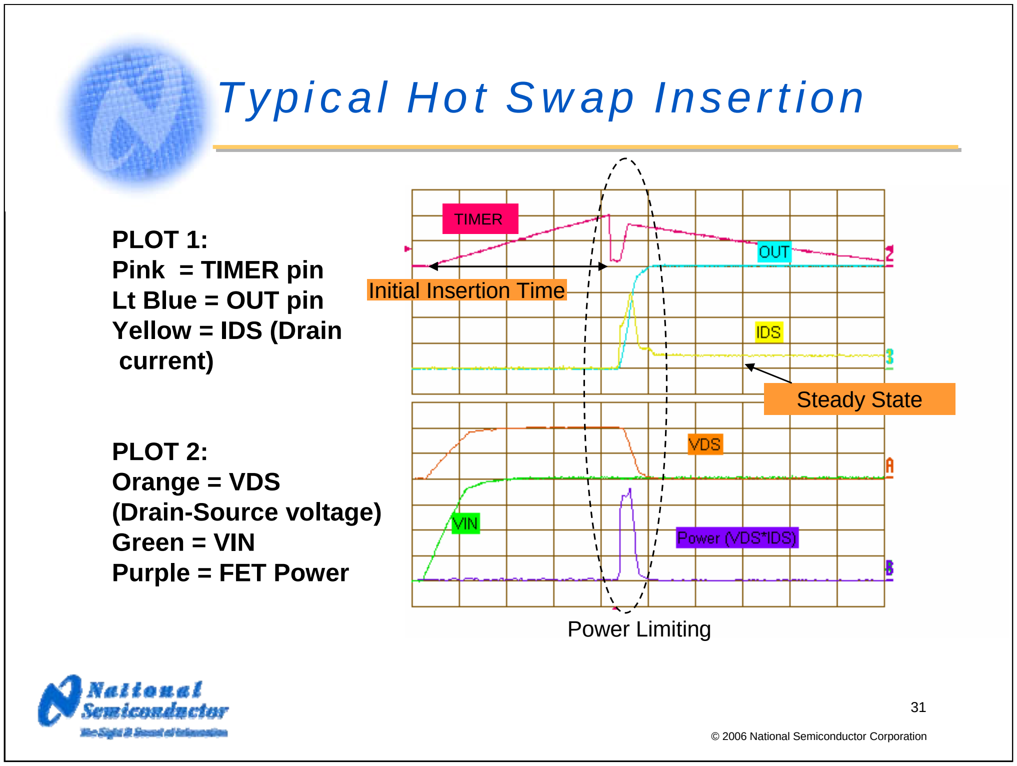
29

Now, recall the curve from prior. We want – we are going to have both a power limit and current limit into a 1,000uF capacitor. We have 80 watts of power and 10 amp current limit. Again, if we have an 80 volt input we will start from one amps at 80 volts Vds and limit to ten amps at eight volts Vds. Anything less than eight volts, the current is limited to ten amps. So, you can see that the LM5069 keeps the MOSFET inside of the SOA and keeps the peak current low.

Now, the following plots are intended to show the versatility of the 5069 and may vary with different layouts and applications, but the overall function of power limiting, current limiting, circuit breaker and initial insertion will be seen.



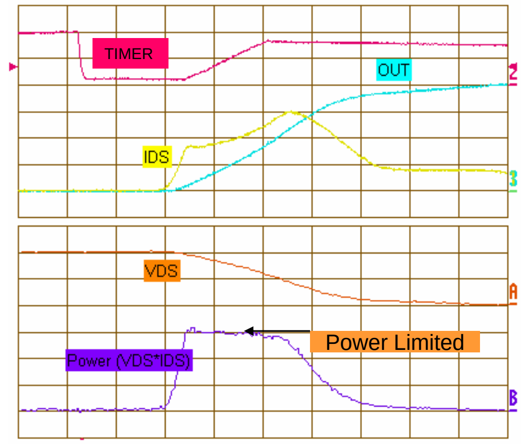
This first slide shows a typical hot swap insertion. What is shown on the top plot is your timer pin, shown in pink; your out pin, shown in light blue; your drain current, shown in yellow. The bottom plot shows the drain to source voltage in orange, your input voltage in green and your FET power in purple. Now, the FET power is a calculation of Ids x Vds. So, you can see that in initial insertion the timer is rising to the four volt fault threshold, but during this time the input voltage is applied to the module, nothing is happening on the out, the Vds is at its maximum and you can see that during this time anything that is running transiently or ringing has the amount of time to subside.

After the initial insertion it will then go in through a limiting mode, shown here as power limit. You can see that the timer rises toward the four volt threshold during this fault condition or limiting condition, but it doesn't reach it because the output has reached its input voltage and goes to steady state.

Power limiting during Hot Swap Insertion

PLOT 1:
Pink = TIMER pin
Lt Blue = OUT pin
Yellow = IDS

PLOT 2:
Orange = VDS
Purple = FET Power



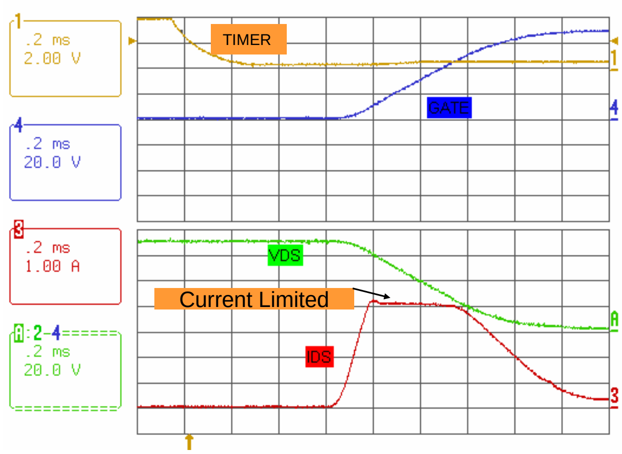
32

This next foil is the zoom in of the power limit. So, you can see that after initial insertion that your Ids current will increase as your Vds decreases in order to keep the power constant. Once it has reached its goal or output, you can see that the Ids current is already decreased and there is no fault and you see the timer start to discharge.

Current limiting during power up

PLOT 1:
Orange = TIMER pin
Blue = GATE pin

PLOT 2:
Green = VDS
Red = IDS



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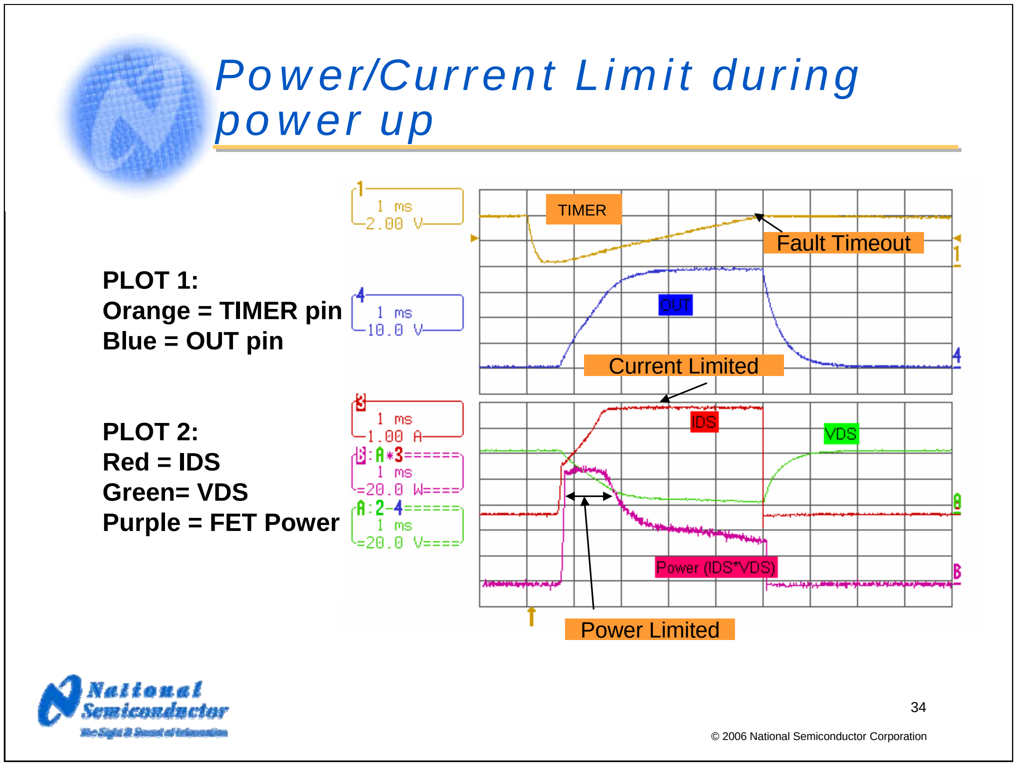
33

This next foil is showing just a current limit after initial insertion. What is shown in orange is the timer pin and this time we've monitored gate in blue. Vds and Ids are shown in green and red respectively. You can see in this case the Vds is decreasing because the gate is being modulated to stay with the current limit. You can see that the Ids stays constant.

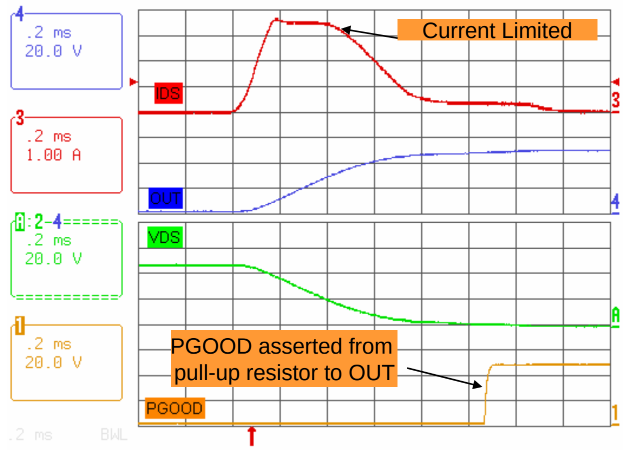


The next foil is showing power limiting and current limiting during power up. So, in this case, after initial insertion you can see that the Ids increases with Vds, shown in red for Ids and Vds in green. But when the Ids tries to increase because Vds is low and tries to maintain a power limit, the current limit will kick in and you get a constant current. Also note that the output has not reached the final voltage during the fault time out. You can see that it has reached its four volt threshold and in this case everything shuts down and your output falls and you go back to a max Vds.

PGOOD function

PLOT 1:
Red = IDS
Blue = OUT pin

PLOT 2:
Green= VDS
Orange = PGOOD pin



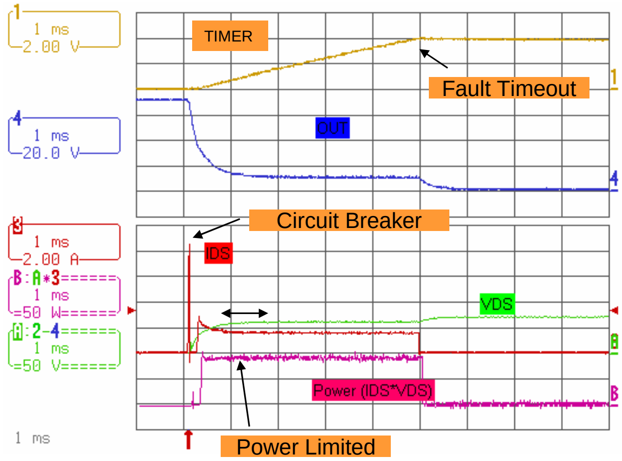
35

This next foil shows the PGOOD function. What is shown in red is your Ids, your output is in blue, your green is in Vds and your orange is PGOOD. Now you can see in this case we current limited, but the whole point is that the output is reaching its input and once it's reached its 1.25 volt away from the input voltage the PGOOD is asserted, because we've turned off the open drain device and there is a pull up from a pull up resistor to out.

Circuit Breaker Limit

PLOT 1:
Orange = TIMER pin
Blue = OUT pin

PLOT 2:
Red = IDS
Green= VDS
Purple = FET Power



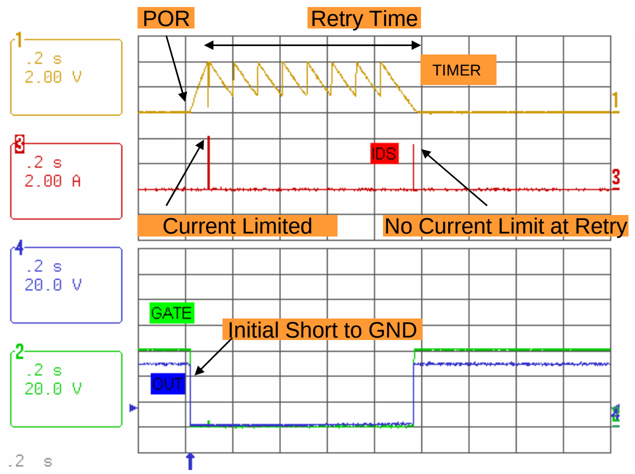
36

Now, this next foil shows that we've heavily loaded the output. So, the top plot shows the timer pin, shown in orange; the output pin, shown in blue; Ids in red, green Vds and FET power in purple. So, when we heavily load it, the Ids current goes beyond any of the limits of current or power limit and hits the circuit breaker threshold. It then shuts off the gate and you can see that the current has fallen to zero. But we've kept the output at this condition and you can see that the current goes into this power limiting mode because since we keep out at a certain voltage the Vds will be constant, the Ids will stay constant to keep the power constant. But again, you can see that it will time out because we've hit the four volt threshold and everything shuts off.

Retry Timer

PLOT 1:
Orange = TIMER pin
Red = IDS pin

PLOT 2:
Green = GATE pin
Blue = OUT pin



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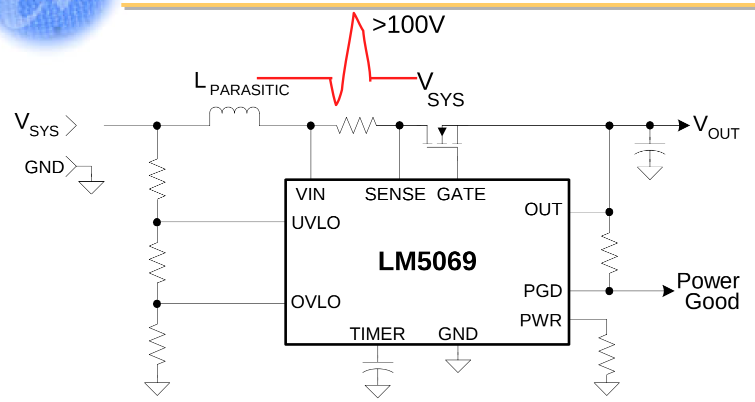
37

This next foil is showing the retry timer. Now, in this case we’ve shorted the output directly to ground. Now instead of going into a circuit breaker function, it goes into a power on reset. So, what is shown in orange is your timer, red is in Ids, the gate pin is in green and your out is blue. So, when we initially short to ground you can see that we go into an initial insertion time and then after the initial insertion, we go into the current limit mode and you see that we’ve timed out. But instead of shutting off for a long time you can see that the timer will toggle between four and 1.25 volts for eight counts and then after the eighth count will retry. Now during this retry time we have taken the short away and you can see now we are going through no current limit and the output is allowed to go up. In this case, this is what is an intermittent short and you can see that we can retry and re-enable without an outside influence.

Now, I've shown that the hot swap controller can limit the inrush current and prevent damage to your module. But another issue will occur when the external FET is suddenly shut off and this is the inductive spike issue.

Inductive spike during fault condition



- Sudden shut off of IDS current causes high voltage spikes on VIN due to the parasitic inductor
- High voltage spikes can cause damage to input of hot swap controller

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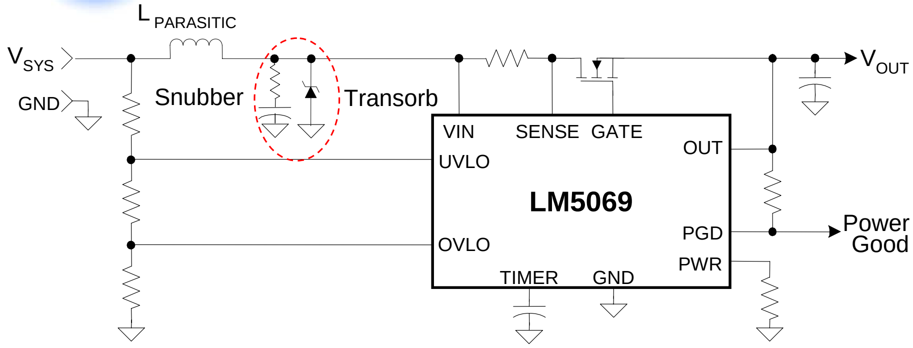
39

What I show here is the same diagram as before, a controller with an external MOSFET, but this time I've added a parasitic inductance, which can be traces, connectors, what not. Now, when you suddenly shut off the gate, let's say because of a circuit breaker threshold, this sudden shut off will cause large spikes on the input line due to the parasitic inductor. Now, these large spikes can cause damage to the input of the hot swap controller because you've gone above its absolute value.

Inductive spike during fault condition



- **Adding a transorb and snubber will help limit the inductive spikes and Vsys transients at the input of the part**
- **The transorb and snubber should be as close as possible to the LM5069**

40

So, in order to reduce these spikes a transorb or snubber or a combination of both will help limit these spikes. The transorb and snubber should be as close as possible to the LM5069 to prevent these inductive spikes.

Conclusion

- **Hot swapping saves time and money by replacing faulty boards on the fly without powering down the backplane**
- **In-rush current due to hot swapping can damage connectors, trace lines, and components**
- **Using an external MOSFET can control the in-rush current, but the MOSFET itself needs to operate inside the safe operating area (SOA)**
- **The LM5069 uses both power and current limit to insure that the MOSFET stays within the SOA and one can confidently hot swap their application**

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41

So, in conclusion I went through the uses of hot swap, specifically in use with a system where down time is not cost effective. Plugging in secondary boards without system shutdown was critical in saving time and money. Simply plugging in a board to the system backplane causes large inrush currents, which can damage the board. The use of an external MOSFET to actively control the inrush current helps prevent damage to the system. However, the external MOSFET itself, if not properly limited, can operate outside its safe operating area.

The LM5069 uses both power and current limit to insure that the MOSFET stays within the SOA and one can confidently hot swap their application.

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More information

LM5069 Product Information:
http://www.national.com/pf/LM/LM5069.html
Power Management Products
http://power.national.com
High-Voltage Switching Regulator Products
http://www.national.com/appinfo/power/hv.html

42

This concludes my presentation. If there is any need for more information, please visit us at our Web site at the following links. Thank you.

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43