

**Built-In SDV Test Pattern Generation  
Improves Video System Testing  
James Mears**

MODERATOR:

Hello and welcome to today's National Semiconductor online seminar. I'm Michelle Miller and I will be your host. Before we begin, I'd like to go over the operation of your seminar interface. Slides will appear in the upper right section of your interface. If you would like the slides to be larger, click the "Enlarge Slide" button. Slides will automatically advance. At the bottom of your interface is an interactive Web browser set to a Web page containing additional resources for this seminar. Questions may be submitted at any time. To ask a question, click the "Question" button on the left, which will bring up an entry window. Enter your question; then click "Submit" to send the question to the presenter. Questions will be answered by email. Finally, National Semiconductor owns and is responsible for all the content in this seminar.

**SLIDE 2**

Today's topic is "Built-In SDV Test Pattern Generation Improves Video System Testing." Today's seminar will be given by James Mears, a member of the technical staff. Welcome, James.

MEARS:

**SLIDE 3**

Thank you, Michelle. Good day. Today I want to introduce you to some of the unique and valuable built-in self-test and test pattern generation features of some of our Serial Digital Video products. My topics today will include the role of built-in self-test and test pattern generation in these Serial Digital Video products. I will talk about some of the products which have built-in self-test and test pattern generation. I will introduce

you to some of the standards and picture formats that are supported by these products. I'll explain how built-in self-test and test pattern generation for Serial Digital Video works in these products. I will discuss how to configure and use the built-in self-test and test pattern generation capabilities in these products. Then we will take a look at some of the product and system applications. Finally, I'll introduce you to some of the design aids and resources that we have to assist you in using these products.

#### **SLIDE 4**

The much simplified digital television data path illustrated here provides a framework from which to discuss how such systems are tested and some of the elements and challenges that can benefit from built-in self-test and internal test pattern generation. From the point where the analog video is converted to digital format through the transmission path to the routing and production switching systems and on to the recording process or transmitter, every point in this digital television chain can benefit from internal self-test.

#### **SLIDE 5**

Digital television products and systems present significant test challenges simply from the nature and size of the data sets involved in creating a picture and also in the parallel and serial data rates that are used by these systems. These systems operate at high serial data rates from 270 Mb per second for standard definition television up to 1.485 Gb per second for high definition. The corresponding parallel data is transported and processed at rates from 27 MHz to 74.25 MHz. The built-in self-test and test pattern generation system should use actual video test data and operate at full system speeds to be effective.

## **SLIDE 6**

The built-in self-test system should take into account the realities of digital TV data. The data is encoded or scrambled in an attempt to avoid data patterns having a significant DC component or runs of ones or zeros. This scrambled NRZ data is then converted to NRZI to reduce the effective transport clock frequency. This in itself causes some problems that scrambling attempts to fix, as we shall see later in this presentation. The data also contains many different and distinct constructs that should be accommodated by the test regimen. For instance, ancillary data sets, which include audio and control information, timing reference signals (these are sync words), the CRC and error detection words or packets, and such things as line numbers in high-definition television data.

Last but not least, the data integrity requirements of digital television systems are very high. Picture quality is paramount and degradation is not tolerated. To combat the problems introduced by the encoding and transmission system, specific stress tests are used to evaluate system elements such as the receiver system phase lock loop and cable equalization. The built-in self-test and test pattern generation system should provide these capabilities, together with the more common non-stressing test patterns.

## **SLIDE 7**

The main features of a built-in self-test and test pattern generation system should be that it uses real digital video for testing. It uses the internal digital video error checking resources of the product. It should operate at the full application speed of the target system. It should fully exercise the device functions. It should be internally self-validating and the data should be available for use in system testing.

## **SLIDE 8**

Some of the advantages that the built-in self-test and test pattern generation systems used in our products have are that the test generation is built into the device itself. No external test generator is needed to test the devices. It enhances Serial Digital Video device and system testing. We have made it simple to use. It is hardware or software enabled. It definitely benefits product development, as I will describe later. It allows a full-speed test regimen and it reduces test time and test cost.

## **SLIDE 9**

The built-in self-test and test pattern generation system must work within the boundaries, methods, and procedures of the digital video industry. The Society of Motion Picture and Television Engineers—or SMPTE for short, the standards organization made up of broadcasters and equipment manufacturers, maintains standards for equipment and procedures used in the production and propagation of the program content. These standards also cover system test. Several such standards are listed here. Digital television data handling makes no provision for error correction due to the real-time nature of the program production and presentation process.

Error detection and correction is an off-line or out-of-service function. Standard definition television uses a method known as error detection and handling, or EDH. This is done on a field and frame basis. High-definition television uses cyclic redundant check characters, or CRCs, with each video line. These methods can be used to good effect if the DTV system incorporates devices with the ability to report the results of the error checking process on a timely basis. The built-in self-test and test pattern generation system must also adhere to the test data standards to be effective. SMPTE standards covering these define specific stressing test data and other related factors.

## **SLIDE 10**

Presently, National Semiconductor manufactures four digital television devices incorporating native code, built-in self-test, and test pattern generation. These you see listed in the slide. The CLC020, which is a standard definition serializer, incorporates built-in self-test and also has an integrated cable driver. The CLC021, another standard definition serializer, has EDH packet generation and insertion capability. The CLC030, a SMPTE 259M standard definition and 292M high-definition serializer can do ancillary data insertion and has an ancillary data FIFO and also an integrated cable driver. The CLC031, a companion device to the 030, is a deserializer which has error reporting capability for both standard and high definition, and ancillary data recovery and an ancillary data FIFO.

## **SLIDE 11**

These devices, the ones that I have just listed for you, produce four standard digital television test patterns. First, a 75% saturation, 8 vertical color bar pattern. This is a non-stressing test pattern that is commonly used throughout the digital video industry. In fact, you probably have noticed it on television. If you watch the evening news, you'll see it on the monitors behind the newscaster occasionally. The next test pattern is a phase locked loop stressing test pattern. This is called a "pathological test pattern" by the video industry. There is next a cable equalizer stressing test pattern, also called an "equalizer pathological." Finally, a flat field black picture which is the foundation on which many other test patterns are constructed. These standard definition patterns are produced for NTSC and PAL systems in standard 4x3 and wide format 16x9 picture aspect ratios. In the high definition products, the patterns support the primary standards, including 1080i and 720p.

## **SLIDE 12**

Next, the slide shows the equalizer stress test. This is a pattern that is used to test the receiver PLL. Recall that the serializer encodes or scrambles the data. Certain colors, when present in large areas of a picture, can result in digital data patterns having undesirable characteristics such as low transition densities or high DC content when sent over the digital data system. These situations and the data that produce them are termed “pathological data conditions” or just “pathologicals” for short. Such color conditions rarely happen in the capture or broadcast of live subject matter. More often they are the byproduct of computer-generated images or matte background generators. These patterns cause stressing of the receiver system. The cable equalizer is particularly stressed by DC shifts that alter the threshold of the receiver input. Well-designed receivers and cable equalizers have wide DC signal voltage handling with DC restoration. This is designed to eliminate the worst effects of such conditions and the resulting data loss.

The specific pathological most commonly used for equalizer testing has a serial data pattern of 19 bits of one polarity followed by a single bit of the opposite polarity. This persists for the length of an entire video line. For NRZI coding, the data can be of either polarity. This serial data causes a large DC shift at the equalizer’s AC coupled input. The pattern is interrupted and the DC is restored during the horizontal blanking interval.

## **SLIDE 13**

The receiver PLL stress test shown here is intended to test the receiver which can also fall victim to unusual data conditions. Certain colors can produce data patterns having low transitioned densities or, if you would, low frequency content. One such color, which is almost seen as black, reduces the effective transport clock frequency by

about four times. The pattern alternates 20 bits of one polarity with 20 bits of the opposite polarity. This pattern persists for the duration of the active video line. Without enough transitions, the received PLL will begin to drift off frequency as the line progresses. If the PLL frequency or phase changes by more than one bit time, there is an almost certain chance of missing individual data bits and possibly of the PLL unlocking entirely. This can cause the loss of one or more picture lines while the PLL regains frequency lock.

#### **SLIDE 14**

Next we'll take a look at some of the features incorporated into the CLC021 SMPTE 259M Standard Definition Serializer.

#### **SLIDE 15**

I've shown here a color bar test pattern to illustrate some of the features of the video raster as it is constructed by the CLC021. This test pattern was originally developed as a product development and test aid. This proved so effective that it was decided to make it available as a means of in-system self-test and as a source of external digital television test signals.

Color bars is probably the most widely used test pattern. It originated in analog television and still finds many important uses in digital television. Color bars is termed a "non-stressing test pattern." It is reasonably well balanced, DC and frequency-wise; hence, it is used for testing jitter and cable transmission distance, among other functions. The built-in self-test and test pattern generation system of the CLC021 generates a color bar signal with standard raster structure.

On this slide I have noted some of the key features and parts of the digital raster that the CLC021 produces. You will note the vertical interval, the End of Active Video point; the Start of Active Video point for each line; the horizontal ancillary interval (or

horizontal blanking, as it is more popularly known); and the active picture area, which is made up of 1,440 samples per line and 487 lines in the case of the NTSC picture. This of course would be interlaced in two fields.

The color gamut produced by the CLC021 is equivalent to the analog version of the color bar picture. Being intended first as a means of testing the device functionality, this color bar pattern differs from the analog and other digital versions by not having digital ramping functions called “transition codes” in the intervals where the luminance or brightness and the chrominance or color signals change from bar to bar. This does not cause device test problems and is generally not a problem for color monitors. It is, however, a problem in situations where the color bar data is applied to digital-to-analog converters. Doing so produces out-of-band frequency products caused by the abrupt code changes.

## **SLIDE 16**

Generating digital television video picture data involves putting together many different data elements. Some of them are illustrated here, such as the End of Active Video data stream called “EAV” and the Start of Active Video or “SAV.” These sequences are also known as “timing reference signals” or TRS. They are the digital equivalent of the vertical and horizontal sync pulses in analog video. These must be present and have the proper coding of the fourth word, known as the “XYZ” word or protection bits, for each particular use in the picture raster. Other data must also be produced like that for the active video line and ancillary data. There must be the correct number of samples per line and lines per frame for each particular picture format such as NTSC or PAL.

## **SLIDE 17**

The CLC021 serializer produces 16 test patterns. Two of these are built-in self-test patterns, the NTSC color bar and PAL PLL pathological patterns. Since the serializer supports both 270 and 360 Mb per second data rates, it can produce both 4x3 and 16x9 raster test patterns. Control of the CLC021's built-in self-test and test pattern generation functions is by hardware control pins. The code for the particular pattern to be used is supplied through the parallel data inputs. The device has an output, which indicates whether the device passes or fails the built-in self-test. The test takes only one frame, either 16.7 or 20ms to run, depending upon which pattern you're using.

## **SLIDE 18**

In order to be truly useful, a built-in self-test should exercise as much of the device as possible. In the CLC021, every circuit is exercised except the power on reset, the first input data register, the output shift register, and the cable drive amplifier. Coverage is 97% of the chip circuitry. The built-in self-test uses the SMPTE standard EDH system as the data-checking mechanism. The EDH system produces several checksums for the active video and the full field. These are compared to values pre-stored in the device for each test pattern. The computed and stored values must agree for the device to pass the test. This assures that all elements are operating correctly, including the data-generating system, error checking system, and the video data processing circuits. If any part is not working correctly, the part will fail the test. This means that the entire system is self-validating. Since the EDH is inserted in the ancillary data space in the proper location, it can be used to exercise other downstream parts of the video system supporting the EDH standard.

## **SLIDE 19**

This slide depicts in much simplified diagram the general operation of the built-in self-test and test pattern generation engine of the CLC021. This same concept is also used in the CLC020 and the CLC030 and CLC031 that will be discussed later on. The system consists of a master controller which accepts commands in the control inputs and keeps track of the current state of the test engine. It directs the use of the pre-stored test data and checksums, which are compared with the computed results and indicate the pass/fail result. The controller also directs the pattern lookup selector, which directs the pattern generator, to select or synthesize the correct pattern elements, packets of data, or individual words in the proper order and quantity. The count of data packets and samples are tracked in a feedback system with the lookup selector. This concept, and the built-in self-test and test pattern generation engine for which patents have been filed, is very efficient in both operation and circuit size, and it occupies only a small area of the chip.

## **SLIDE 20**

Coverage achieved by the built-in self-test system is extensive and includes these major systems: the PLL system, the data registers, the scrambling and encoding system, the timing reference signal detection, error detection and handling system, the ancillary data system, the chip control system, and the built-in self-test and test pattern generation data and checkwords themselves.

## **SLIDE 21**

The basic control of the built-in self-test and test pattern generation system of the CLC021 uses its normal control and data inputs. The codes of the test patterns are applied to the lower four parallel data inputs, D0 through D3. The upper inputs are ignored when in test pattern generation mode. The clock is applied to Pclk as would be normal. The test

pattern generator enable input is used to begin and end the test or to turn on and turn off the test pattern generator. The pass or fail indication is via the test output. The operation of the TPG can be automated by feeding the lock detect output back to the TPG enable input so that when the PLL locks, TPG will start automatically. The test data is available on the serial data outputs. The built-in self-test patterns in this device are the NTSC color bar pattern and the PLL PAL pathological pattern.

#### **SLIDE 22**

Using the built-in self-test and TPG feature in an application involves adding multiplexing for the code inputs to the parallel data input. This could be done using a multiplexer or tri-state drivers. Also, the TPG enable will be controlled either directly from the system host control system or connected to lock detect during this mode of operation. Pclk would be the normal clock used for input of parallel data. The host system should monitor the test result on Test-Out.

#### **SLIDE 23**

Next we'll take a look at the CLC030, the SMPTE 259M and 292M standard and high-definition serializer.

#### **SLIDE 24**

Here I've shown again the color bar signal. You'll notice that it is a wide format picture, which is what is used in high-definition television broadcast. The active picture area consists of 1,920 samples per line and 1,080 lines in this particular example, which is a SMPTE 274M picture standard or 1080i, in other words. Again, I've shown the vertical interval, the vertical switching interval, the End and Start of Active Video, and the horizontal ancillary interval.

The CLC030 serializer also incorporates a similar built-in self-test and test pattern generation system to that used in the CLC021. The test system has been expanded to include the SMPTE 344M, which is a 540-Mb standard, and the HD formats. In the HDTV realm, the same test patterns are used as in standard definition. The major difference, as I've shown here, is the larger size of the raster, which means more data; in this case, something over 9 MB of data per picture. Generating the test patterns and the data algorithmically, as this device does, is economical both of storage and of chip area.

#### **SLIDE 25**

The HD video data sequence is similar to the SD data sequence. The major differences beyond the longer active video line length are that the luma and chroma data streams are treated as separate data entities and interleaved to produce a combined stream. This means that the TRS character sequences are duplicated, as can be seen here in the EAV and SAV. I've noted the chroma streams with a "C" and the luminance streams with a "Y" in each of the data words illustrated. Also, line numbers and CRC checkwords are appended to each line after the End of Active Video. The ancillary data space is similarly duplicated in both luma and chroma data. Ancillary data such as audio is carried in the chroma channel. However, two audio control packets are carried in the luma channel.

#### **SLIDE 26**

The CLC030 offers the same set of basic test patterns as the CLC021. These patterns are now available in all of the CLC030's supported formats and rates. The built-in self-test patterns for standard definition are the same as those of the CLC021. All of the HD formats are built-in self-test patterns by virtue of the use of the CRCs on every

line. In addition, the CLC030 features a means of optionally adding transition codes in the luma and chroma changes in color bars. This functions for all formats and rates.

The built-in self-test and test pattern generation system of the CLC030 is controlled either by software through its control register set or a combination of hardware and software, as many of the TPG controls can be mapped to the user configurable I/O bus if desired. I want to point out that since the device can recognize the format, a function of the TPG system, it can easily validate if the incoming data has a valid format. This is useful when creating video data from scratch or from edited and combined source data. It tells you when the format is correct or not.

#### **SLIDE 27**

The CLC030 and its companion deserializer, the CLC031, use common core logic that comprises both a deserializer and a serializer in a loop configuration. This gives some unique advantages to the built-in self-test and test pattern generation system operation. Data is inserted in the serializer, scrambled, and again deserialized to original form. This enables a more complete test of the system than previously possible. In the CLC031, this permits the test pattern generator to operate without an external clock or data source.

#### **SLIDE 28**

This functional diagram of the CLC030 indicates the major data and control path elements tested by the built-in self-test and test pattern generation system. Of course, the major objective of any built-in self-test is to test the device for operational integrity, using as much of the device itself as possible.

## **SLIDE 29**

I've mentioned transition coding in connection with the color bar test pattern. This technique was developed for the CLC030 and 031 to make it more friendly to systems using digital-to-analog conversion. The transition coding consists of adding a sequence of increasing or decreasing digital data code values instead of abrupt code changes in the luma and chroma data where these change for each new color bar. For example, the luminance value changes from 3AC hex to 284 hex when going from the white bar to the yellow bar. Transition coding adds a five-step sequence, which gradually decreases the luma code value from 3AC to 284. Similar sequences are inserted in both the chroma data streams. These code transition sequences are similar to but not identical to those used in some other test patterns, but the beneficial effect is the same. This technique of transition coding is also called the "video pattern generator filter" in connection with the CLC030 and 031.

## **SLIDE 30**

The degree of test coverage afforded by this technique is extensive. It includes the PLL system, the data registers, the scrambling and decoding system, the timing reference and format detection system, the CRC or the EDH system, the video data FIFO, the ancillary data insertion system, the control system and the control register set, and the system master controller functions.

## **SLIDE 31**

Operating the built-in self-test and test pattern generation system of the CLC030 is fundamentally a three-step process. To set up the built-in self-test and test pattern generation system, one or two registers need to be loaded. For these control register write operations, both the ancillary control bar and read/write bar lines will be held low. Aclk

will be toggled to load each register address and data word. First, the video pattern generation filter can be enabled if desired. This is done by first loading into the device the address of the register where the VPG filter enable bit resides. The upper two bits of register address are always 00 binary. Then the data to enable the video pattern generation filter is presented and clocked into the selected register. In this case, it is bit 5 of the test 0 register. The upper two bits of a control data word are always 11 binary.

Second, the address of the test pattern select register is clocked in. Then the code of the desired test pattern is clocked into the register. In this example, the test pattern is the BIST test pattern for SMPTE 125M, the 270-Mb NTSC color bar pattern. Since the test is to be enabled by hardware control of a TPG enable input, which is I/O bus bit 7, we next set this input high and toggle Aclk to register the enable. The pass or fail indication appears on I/O bus bit 6, the pass/fail output. The test data of course is available to the system on the serial data outputs.

### **SLIDE 32**

The built-in self-test and test pattern generation system of the CLC031 deserializer operates almost identically to the CLC030. In the example shown here, we will do a few extra steps which re-map the TPG enable control and the pass/fail indicator output to the user I/O bus. These operations are performed in a manner identical with the previously described loads of addresses and data to the TPG system registers. To remap the TPG enable to I/O bus bit 7, the register address, 16 hex, is first loaded, followed by the data corresponding to the TPG Enable's map code 328 hex. Next, the pass/fail indicator bit is mapped to I/O 6 by writing 31D hex to register 015 hex. Step three enables the VPG filter, as was done in the CLC030 example. Step four sets up the device to output a SMPTE 274M high-definition color bar signal. This is done by writing 323

hex to register 00D. Finally in step five, the TPG is turned on by bringing the TPG enable input high and clocking this command in using Aclk. The pass/fail indicator will show the test result. Notice that no video clock is used in this instance. The 27 MHz reference clock, used for the PLL and clock data recovery system, will take control and lock the part into operation. The parallel data and its parallel write clock will be output on the video data buses and the Vclk.

### **SLIDE 33**

Next I'd like to take a look at some of the product and system applications for built-in self-test and test pattern generation and where this has been official.

### **SLIDE 34**

The serializer products I have just described can bring added utility to a variety of products and applications. Cameras and camcorders are two such types of products where having built-in self-test and test pattern generation provide added utility. The built-in self-test can become an important part of a power-on diagnostic routine to see if the entire camera or camcorder is working correctly. The test patterns also find utility both in internal and external test applications. Naturally, the serializers provide, in addition, two cable driver outputs in this application.

### **SLIDE 35**

In production control systems, routers and switchers, the serializer and deserializer products find a place. Not only is diagnostic testing possible, but the test patterns can replace or augment other test signal generation resources in the television plant. Color bar and black raster signals are internally available that can be used throughout the television system. A test-before-connect system can be used to verify correct path operation in the production center or router before the path is completed. An

alternate path can then be selected automatically if the original path proves to be unserviceable.

### **SLIDE 36**

A common test regimen used to test digital television systems is to add cable in the system to test its tolerances and limits. This type of testing can be performed without external test resources if both the CLC030 and CLC031 are part of the system. Shown in this diagram is one possible application in a production control switcher. Here the CLC030 acts as the serial signal generator and the CLC031 as the error indicator. The CRC and EDH system of the CLC031 deserializer are used as the receiver detector which monitors the incoming data for errors. The test path goes through the switcher and to an external path through the television plant. As cable is added to the path, the point at which errors begin to occur can be monitored using the CLC031 CRC error detection system. If one of the stressing test signals such as the equalizer pathological is used, the response of each receiver input of the switcher or other system in the path can be assessed. If errors occur under this condition, the result can be checked by changing the test pattern of the CLC030 to a non-stressing pattern such as color bars or by enabling its internal pathological dithering system.

### **SLIDE 37**

Several portable and fixed-mounted test pattern generators on the market today use the CLC021 or CLC030 as the major test pattern generator component. The versatile CLC030 serializer and CLC031 deserializer also find application in a variety of other digital video test appliances such as video signal and data analyzers.

**SLIDE 38**

Even such systems as television transmitters can benefit from internal built-in self-test and test pattern generation. During installation, checkout, acceptance tests, maintenance, and even normal operation the test pattern generator is a handy utility. When the ancillary data handling capability of the CLC030 is used, embedded audio tone generation is also possible.

**SLIDE 39**

National Semiconductor offers extensive assistance to video engineers through our application support group. We have also developed design aids specifically to assist the video engineer in his design tasks. The Serial Digital Video and Interface RAPIDESIGNER© Sliderule shown here solves design tasks such as application of the CLC016 re-clocker. It does transmission line design, including differential lines, return loss calculations, Thevenin termination, and vector impedance calculations. Other sliderules specifically for transmission line design are also available. Our extensive application note library and frequently asked question library contain additional information on these and other products. I invite you to come to [www.national.com](http://www.national.com) and make use of these valuable resources.

**SLIDE 40**

In addition to our factory applications engineers, our customer response center is staffed with capable engineers to assist you with your technical questions or direct you to additional support.

**SLIDE 41**

I'd like to thank you very much for attending our seminar on "Built-In Self-Test and Test Pattern Generation," and have a nice day.

MODERATOR:

Thank you, James. That concludes our presentation. I'd like to invite our viewers to please fill out and submit the survey form, which should be appearing on your screen shortly. Your answers to this survey will help us in the development of new products as well as future seminars. Thank you, everyone, for viewing the seminar, "Built-In SDV Test Pattern Generation Improves Video System Testing," brought to you by National Semiconductor and Yahoo Broadcasts.

(End of Presentation)