

The Xilinx Virtex™-5 and Altera Stratix® III are families of advanced FPGAs based on 65-nm cores that combine various platforms and speed grades enabling a high level of performance and flexibility. This article discusses FPGA power supply prerequisites as needed by the system designer in terms of the multiple voltage rail and current level requirements, output sequencing, and startup characteristics. Following, a power supply solution based on National Semiconductor's LM1771 and LM3880 is designed that combines high performance, power density and efficiency.

### FPGA Power Supply Requirements

The Virtex-5 or Stratix III FPGAs generally require at least two different voltage rails. The recommended Virtex-5 core voltage, designated  $V_{CCINT}$ , is  $1.0V \pm 50$  mV while the Stratix III core rail, denoted  $V_{CCL}$ , can be selected as  $0.9V \pm 40$  mV or  $1.1V \pm 50$  mV. Depending on the I/O standard being implemented, the Virtex-5 I/O voltage supply,  $V_{CCO}$ , can vary from 1.14V to 3.45V. Thus,  $V_{CCO}$  voltage rails of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V are feasible. Similarly, Stratix III specifies that the I/O voltage,  $V_{CCIO}$ , can vary from 1.14V to 3.15V, yielding 1.2V, 1.5V, 1.8V, 2.5V, and 3.0V as voltage rail possibilities.

Furthermore, Xilinx defines an auxiliary voltage,  $V_{CCAUX}$ , which is recommended to operate at  $2.5V \pm 5\%$  to supply FPGA clock resources. Altera defines additional rails specified for the digital and analog PLL sections, I/O pre-drivers, differential clock inputs, and such. It is required that the power supplies transiently handle larger currents during startup with relatively lower static and dynamic currents during normal operation. The power-up ramp time specification for each voltage rail is 0.2 ms to 50.0 ms for the Virtex-5 and 0.1 ms to 100.0 ms for the Stratix III.

### FPGA Power Supply Design Outline

This proposed FPGA power supply solution is aimed at the Virtex-5 FPGA. A corresponding power supply strategy can be implemented for the Stratix III with subtle changes considering the aforementioned differences.

The power-on sequence recommended by Xilinx is  $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$ . Although any monotonic power-on sequence is tolerated, use of the recommended sequence allows Xilinx to define the minimum inrush current required from the FPGA core, auxiliary and I/O supplies - denoted  $I_{CCINTMIN}$ ,  $I_{AUXMIN}$ , and  $I_{CCOMIN}$ , respectively - to ensure correct power-on and configuration. The solution uses three National Semiconductor LM1771 PWM controllers with power-up and power-down of the individual voltage rails sequenced by a National Semiconductor LM3880 power sequencer.

The LM1771 block diagram with typical external components is presented in *Figure 1*. The LM1771 is an efficient buck converter switching controller available in MSOP-

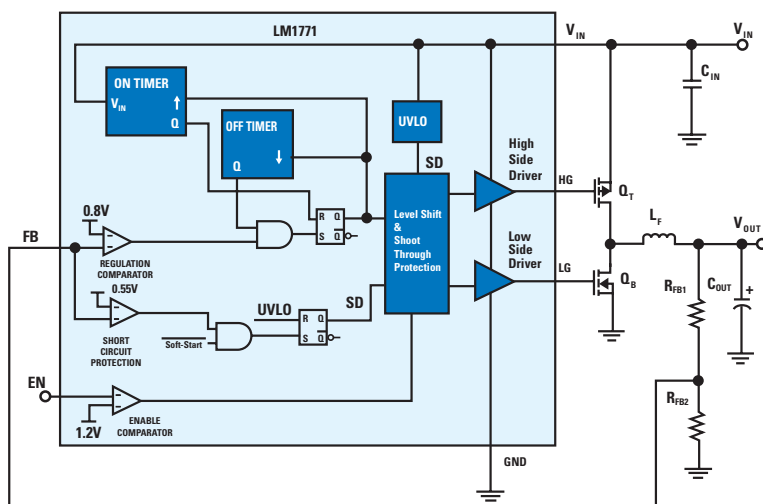


Figure 1: LM1771 DC-DC Buck Stage with COT Control Architecture

8 and LLP-6 packages and capable of converting an input voltage between 2.8V and 5.5V into a regulated output voltage as low as 0.8V. It drives an external high side PFET and low side NFET and utilizes a constant on-time (COT) control architecture which eliminates the need for an error amplifier and external compensation components. Thus, extremely fast transient load current response is possible. Additionally, the LM1771 features a precision enable pin to facilitate supply sequencing and/or flexibility in setting the operating range of the power supply.

Three LM1771 timing options - designated S, T and U in the part numbering specification - are available which translate to three possible frequency options for a given output voltage. For a given timing option, the switching frequency is independent of input voltage level as the controller input feed-forward feature varies high side switch on-time as a function of input voltage to maintain constant volt-seconds at the switch node.

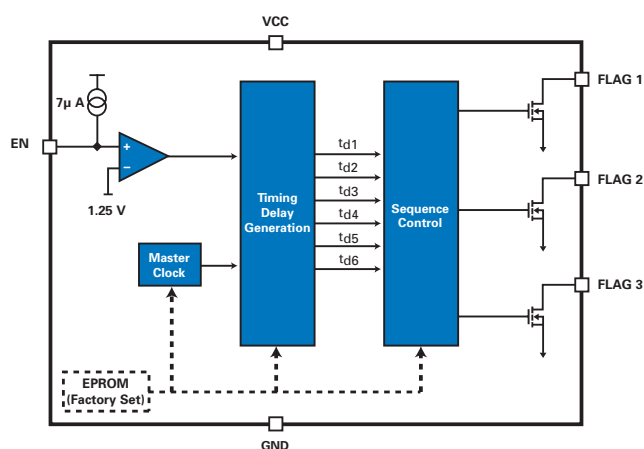


Figure 2: LM3880 Sequencer Block Diagram

By virtue of the small-sized package options, the LM1771 allows for a complete power supply design to occupy very little PCB real estate without sacrificing efficiency or performance.

The LM3880 sequencer block diagram is presented in *Figure 2*. It is available in a SOT23-6 package and it has three open-drain flag outputs which allow control of the three LM1771 enable pins. Upon enabling the LM3880, the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch-up conditions. Standard timing options of 10 ms, 30 ms, 60 ms and 120 ms are available. Additionally, the LM3880 is factory programmable to attain customized timing options combined with six possible power down sequences.

### FPGA Power Supply Implementation

The LM1771 and LM3880 based power train schematic is shown in *Figure 3*. For this design, the three buck regulator channels are capable of delivering maximum continuous load currents of 5A,

3A and 3A ( $I_{CCO}$ ,  $I_{CCAUX}$ , and  $I_{CCINT}$ , respectively). The I/O voltage is set at 3.3V, but can be easily varied by modifying one of the feedback resistors. The core and auxiliary rails are set at 1.0V and 2.5V, respectively.

The core, auxiliary and I/O regulators use the LM1771S, LM1771T and LM1771U controllers which yield switching frequencies of 606 kHz, 758 kHz and 500 kHz, respectively. Each supply has its own input filter capacitor located as close as possible to the p-channel and n-channel buck and synchronous power FETs. Additionally, a small input bypass capacitor is placed local to each LM1771 IC.

The output filter capacitances on the core and I/O supplies are tantalum based and chosen to present the necessary Equivalent Series Resistance (ESR) to maintain sufficient in-phase ripple at the Feedback (FB) pin. A feed-forward capacitor from  $V_{CCO}$  to the FB pin increases the magnitude of the ripple seen by the LM1771. The output filter capacitance of the auxiliary voltage regulator is ceramic based to minimize the noise level of this rail. A resistor capacitor current sense network across that channel's filter inductor creates a triangular waveform which is ac coupled to the FB node. This circuit can also be utilized in the core and I/O channels if tantalum capacitors are deemed unsuitable and/or low ESR ceramic capacitors are required either local to the regulator or downstream adjacent to the FPGA.

The filter inductors are designed for large current handling capability with low DC and AC effective resistance to maximize efficiency. The inductance value is conditioned to attain peak-to-peak ripple current of approximately 30% of the rated load current. Further, it is desirable to choose a relatively soft saturation characteristic to handle short duration high current transient events in excess of the rated load current.

TSOP-6 packages are used for the power FETs in the auxiliary rail supply while SO-8 FETs are implemented for the I/O channel regulator. The core voltage supply, given its low duty cycle operating point, has a high side TSOP-6 FET and a low side SO-8 FET.

The LM3880 30 ms timing option, designated -1AB, is recommended. External pull-up resistors are connected to each open-drain flag output.

### FPGA Power Supply Performance

The efficiency of the I/O channel, operating independently at 5V input, as a function of current is shown in *Figure 4*. Overall conversion efficiency with the three regulators operating at full load, including LM3880 related bias power, is 90.5%. This constitutes a total output power of 27W with 2.85W dissipation. *Figure 5* demonstrates the sequenced monotonic startup characteristic as controlled by the LM3880. The time delay between respective startups is 30 ms. ■

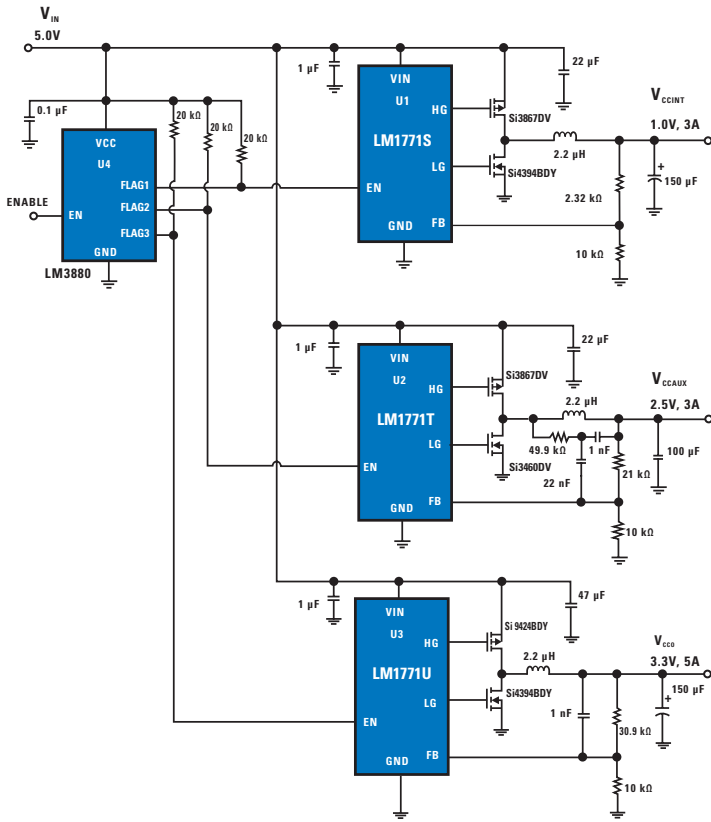


Figure 3: Virtex-5 FPGA Power Train Schematic

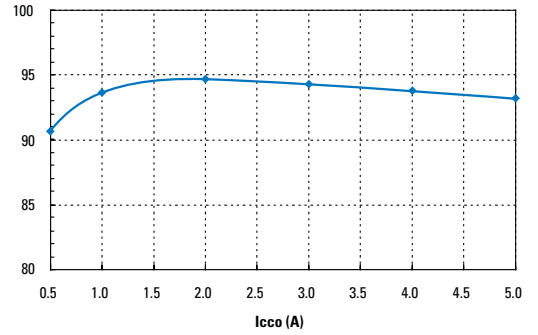


Figure 4: I/O Channel Efficiency vs. I<sub>cco</sub>; VIN = 5.0V

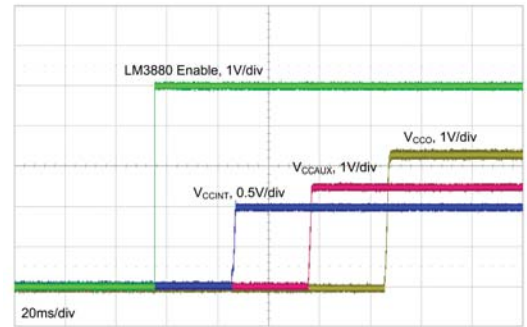


Figure 5: Sequenced Startup Characteristic; VIN = 5.0V

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